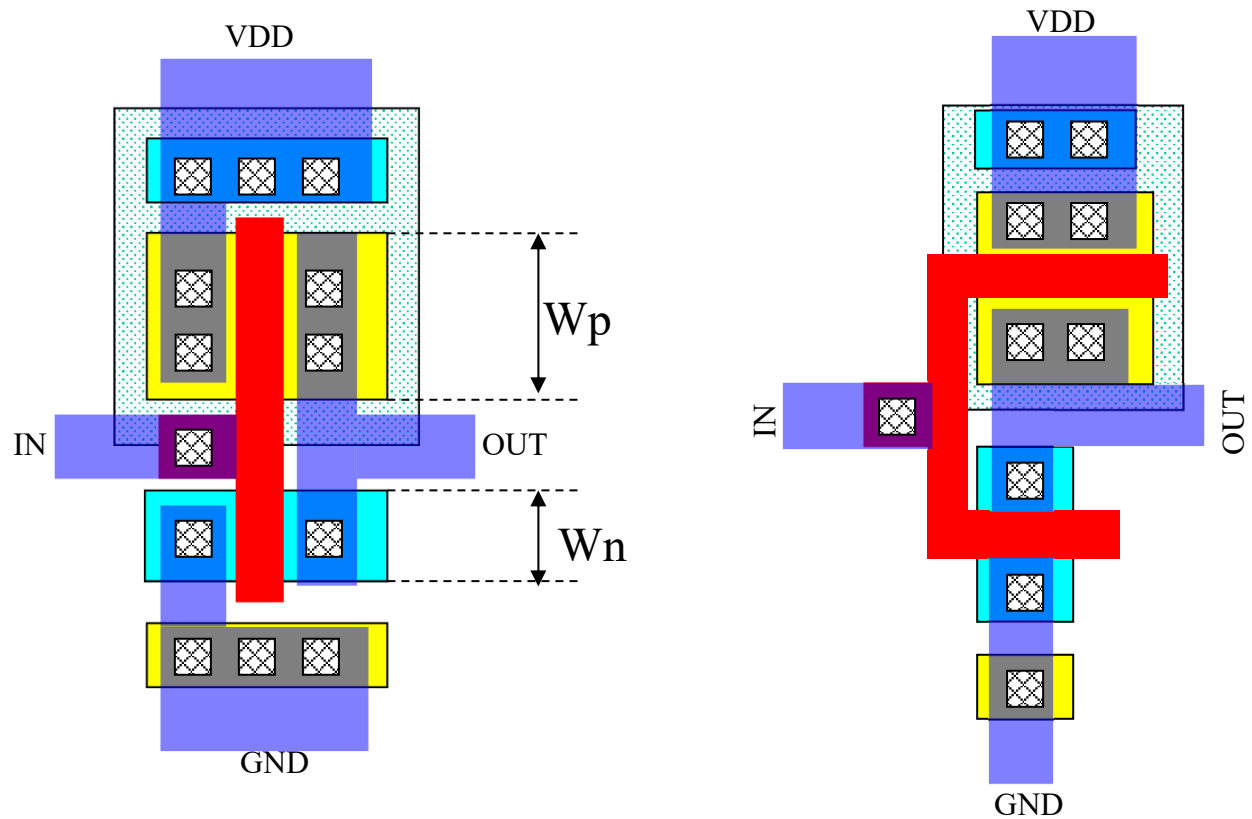



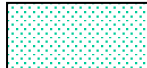


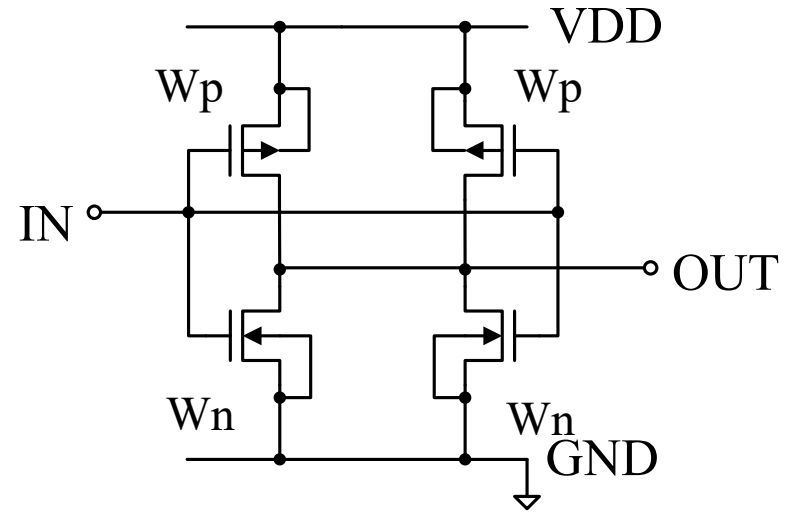
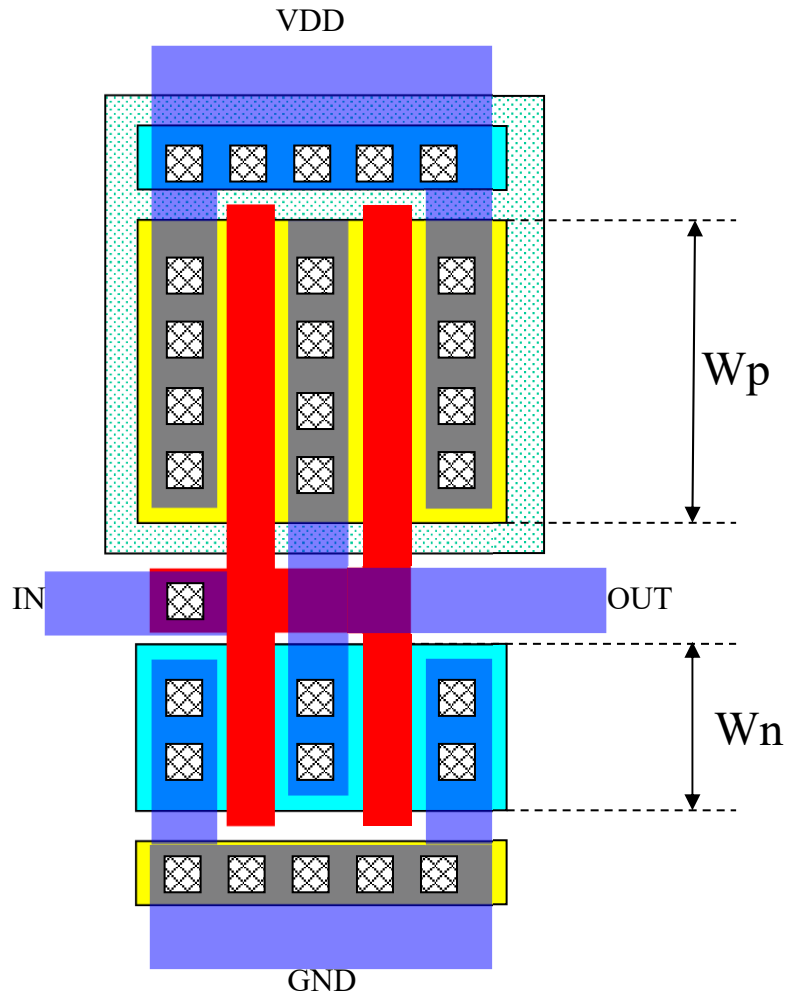


Layout example of inverter

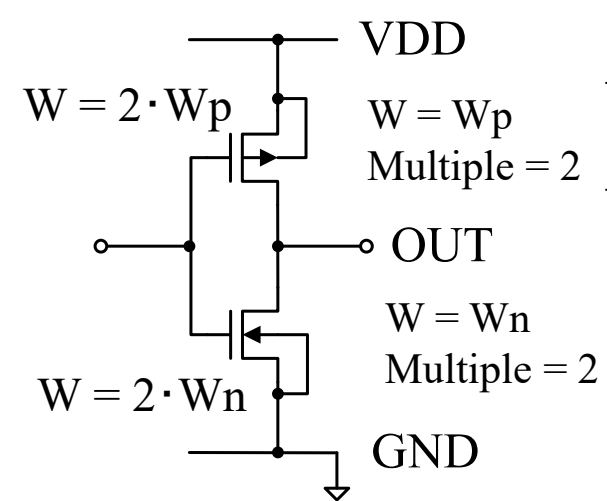


-  n+ active
-  p+ active
-  Gate Poly
-  n-well
-  Metal
-  Contact

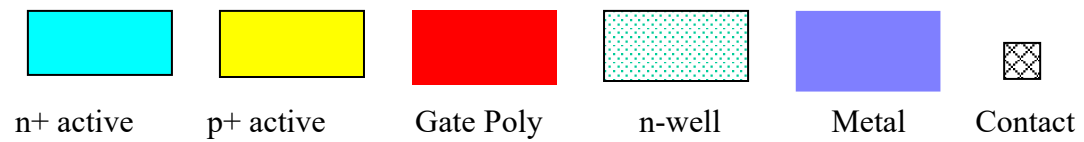
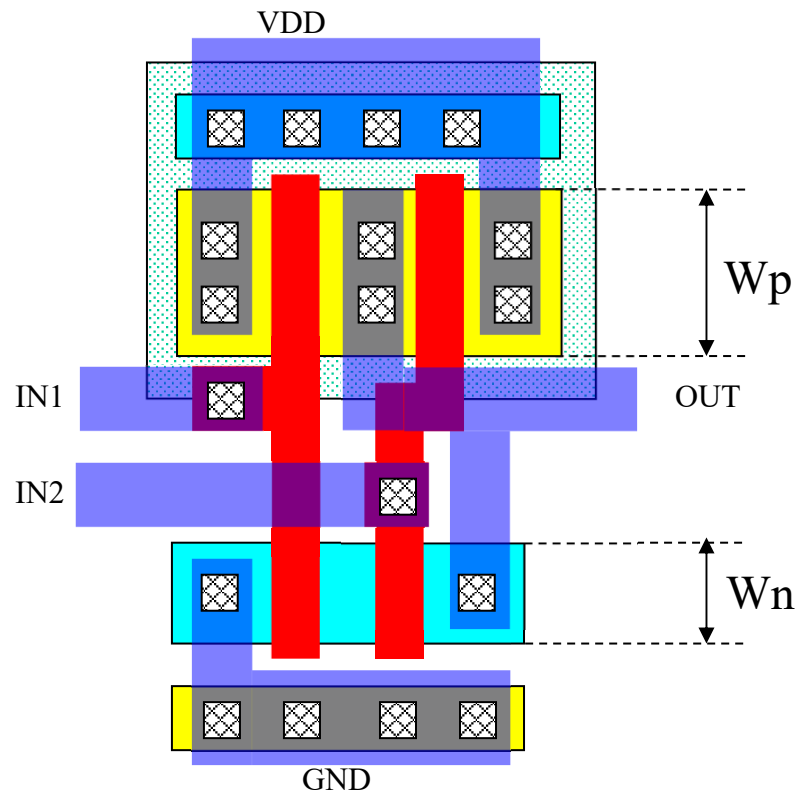
Layout example of inverter (Large W/L)



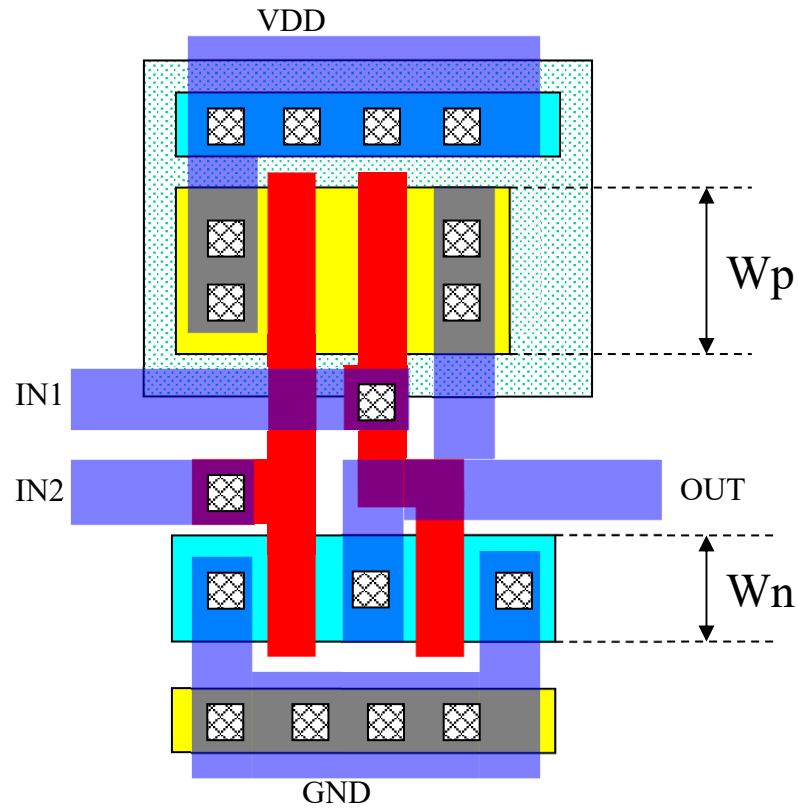
|| Notation in schematic




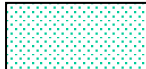




Layout example of NAND gate

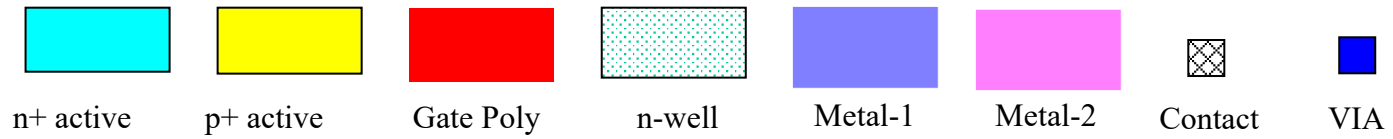
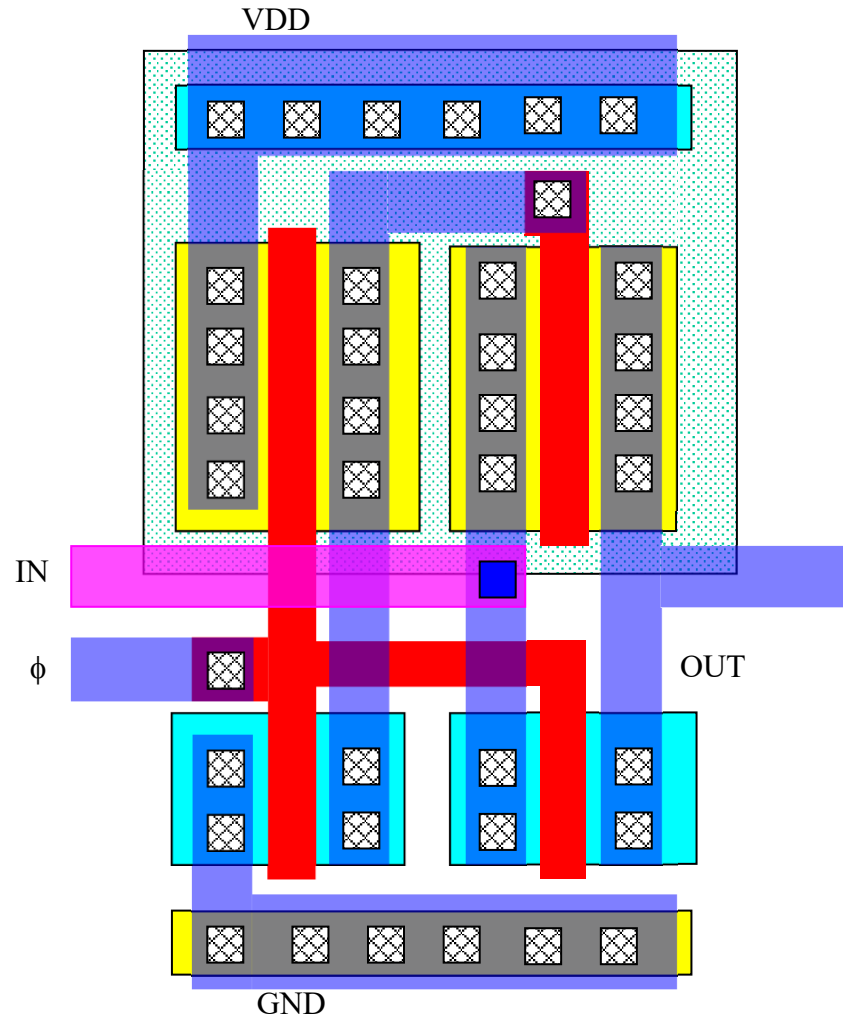


Layout example of NOR gate

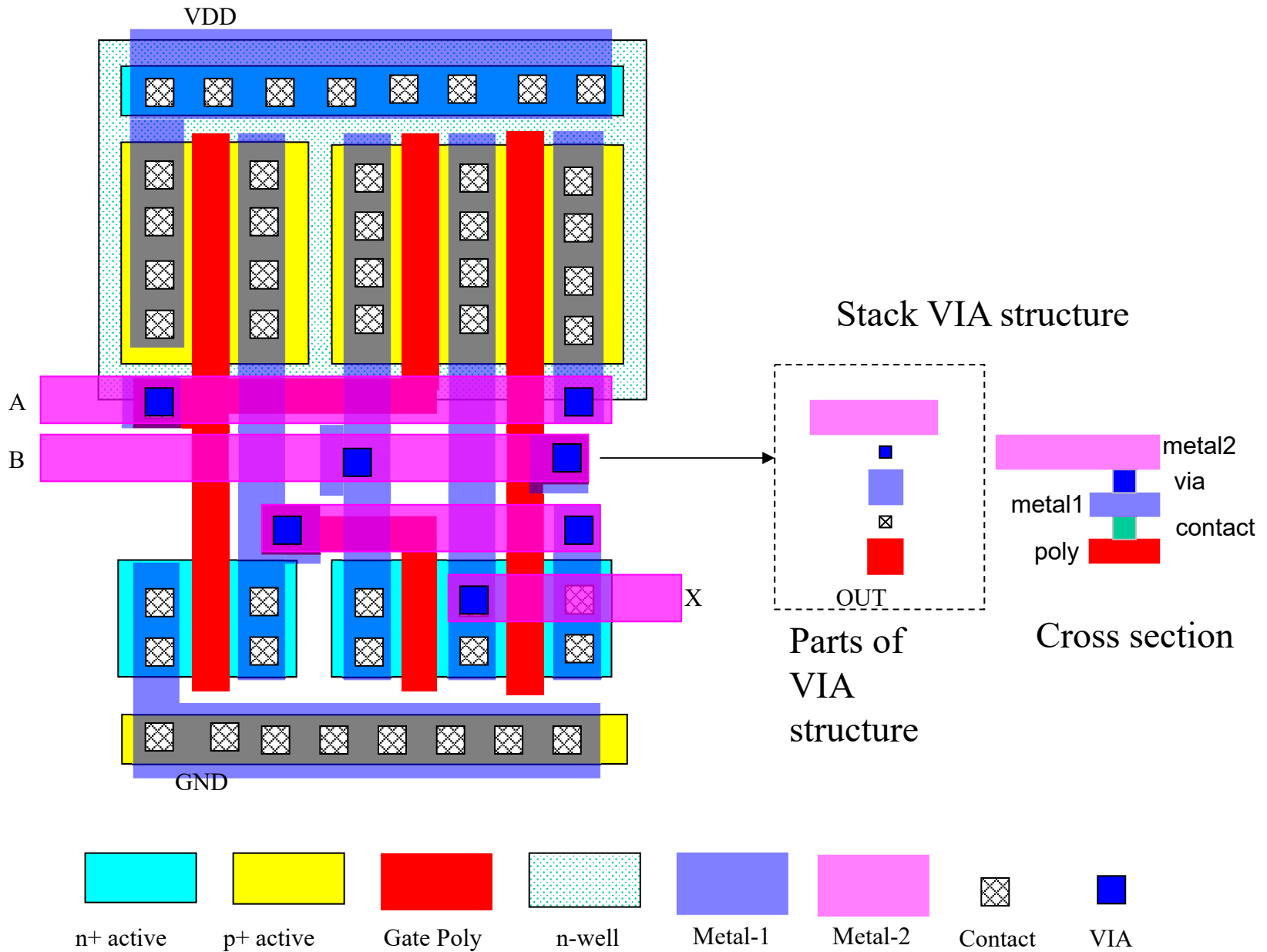


					
n+ active	p+ active	Gate Poly	n-well	Metal	Contact

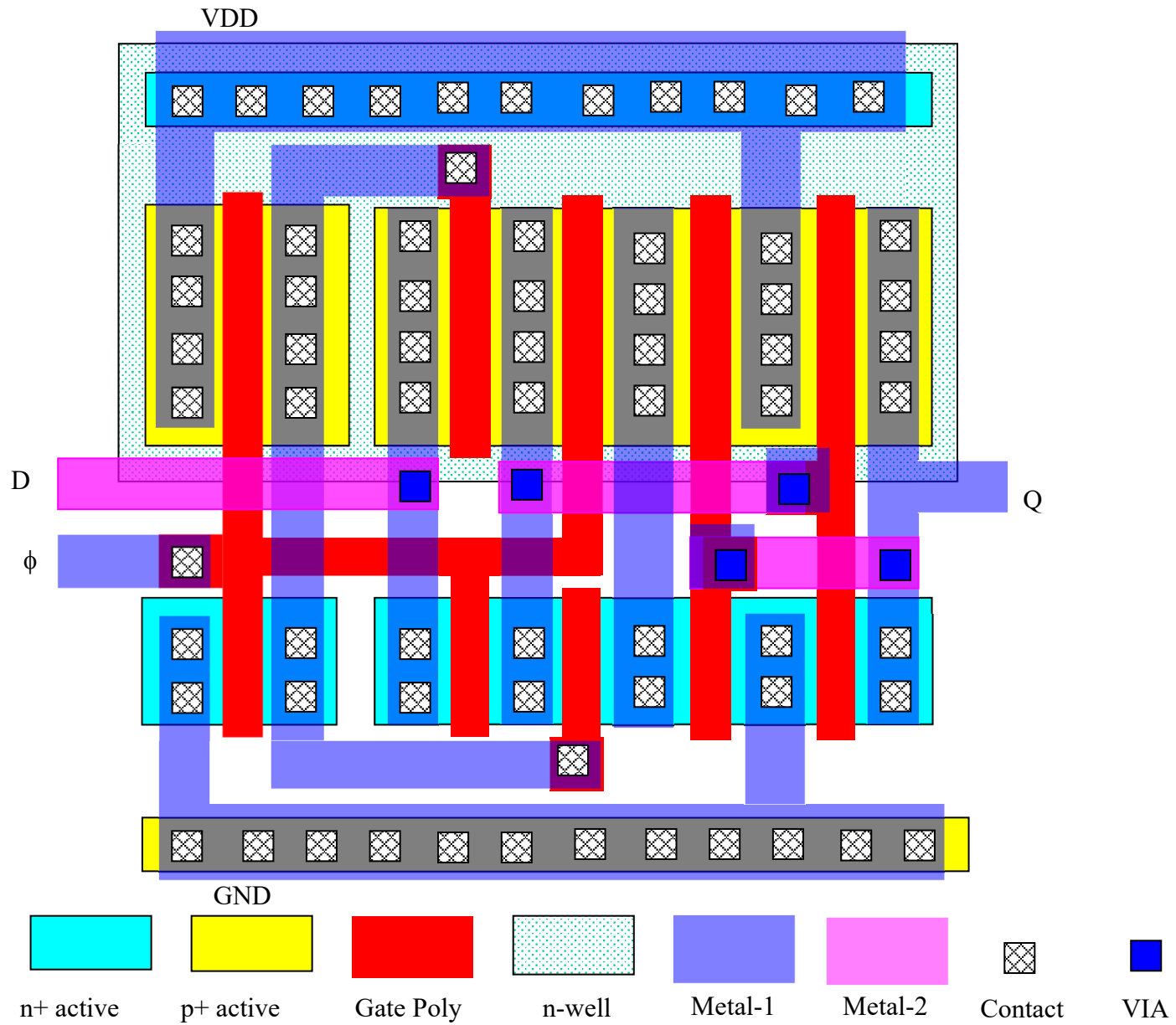
Layout example of TG



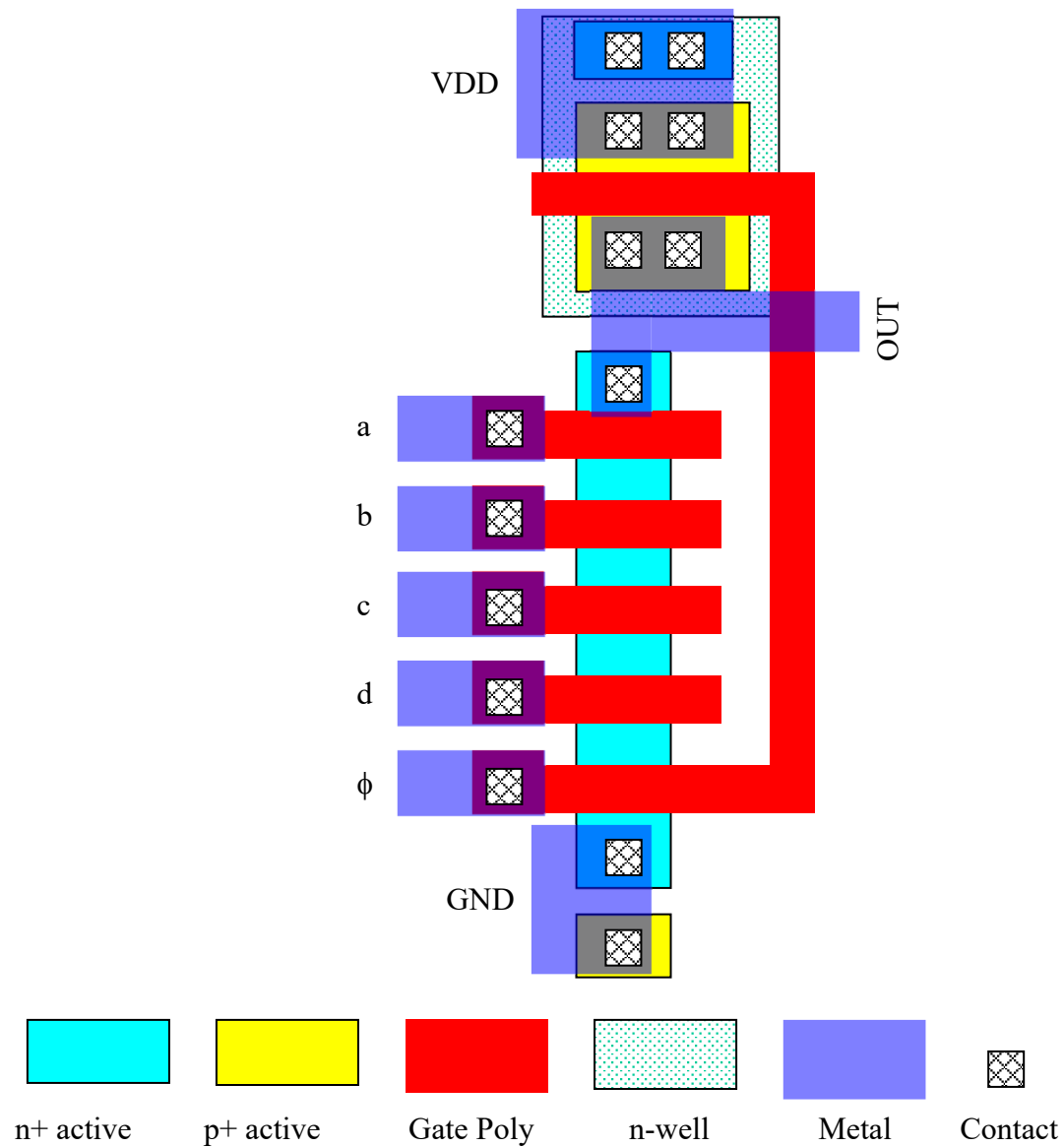
Layout example of EXOR gate



Layout example of D-latch



Layout example of NAND designed for dynamic CMOS logic



Layout example of D-FF designed for dynamic CMOS logic

