6.2 Power consumption

Analysis of power consumption and clock frequency

Power consumption in CMOS logic

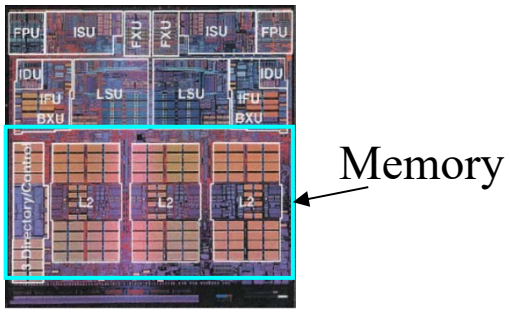
Classification of current path

a. $P_{cd}(W)$ by a charge-discharge current
b. $P_{dp}(W)$ by a direct path short circuit current
c. $P_L(W)$ by a subthreshold current, pn junction leakage current, gate tunneling current

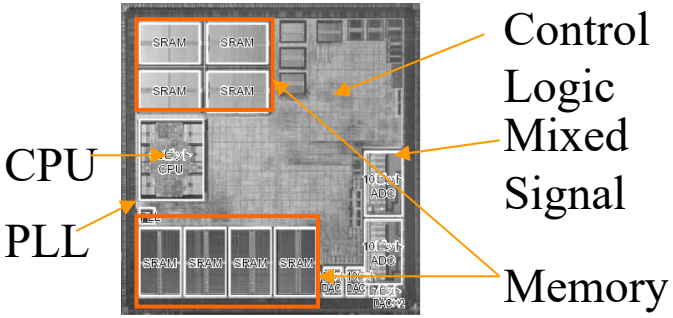
Classification of operating mode

a. Dynamic power consumption $P_{at}(W)$
b. Static power consumption $P_{st}(W)$

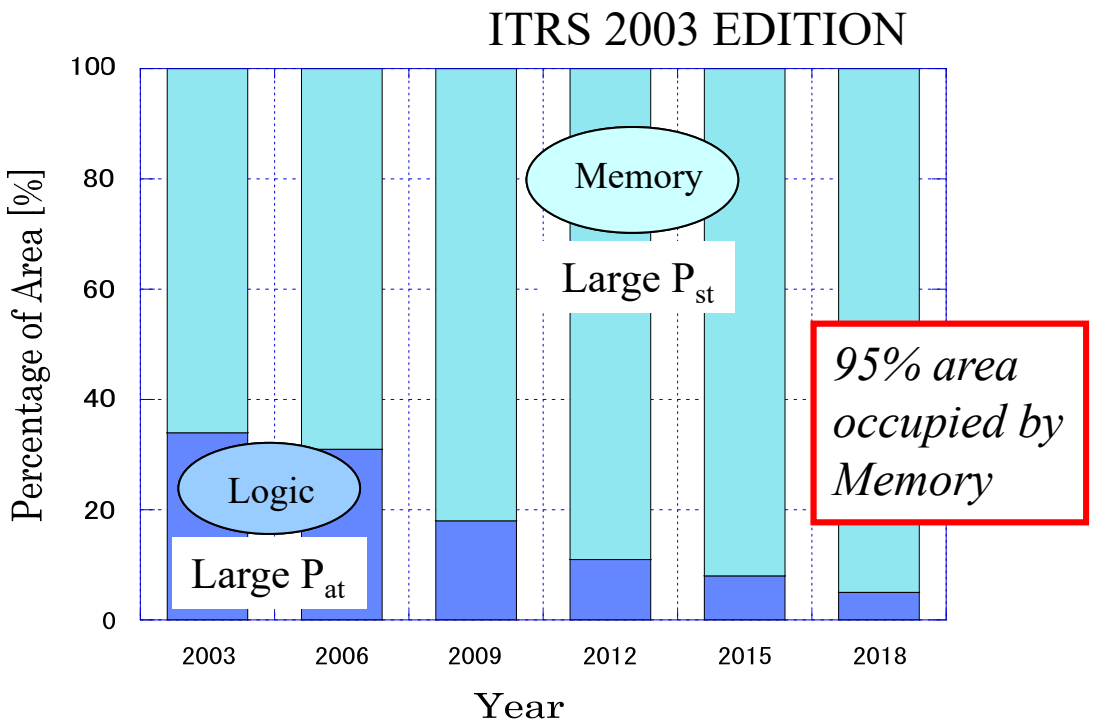
Trends of power consumption



IBM Power 4 (Dual core)



Toshiba 5GHz WLAN



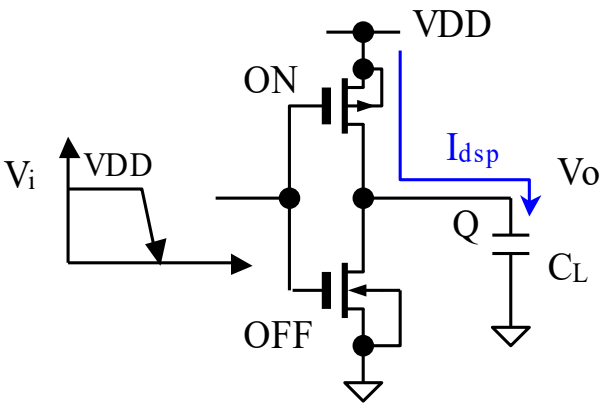
The static power consumption by memory is increasing with the generation.

Charge-discharge current (Charge)

Charge current and output voltage

$$Q = C_L \cdot V_O$$

$$I_{dsp} = \frac{dQ}{dt} = C_L \cdot \frac{dV_O}{dt}$$



Energy consumption by p-ch MOSFET

$$E_C = \int_0^\infty I_{dsp}(t)\{VDD - V_O(t)\}dt$$

$$= VDD\int_0^\infty I_{dsp}(t)dt - \int_0^\infty I_{dsp}(t)\cdot V_O(t)dt$$

$$= VDD\int_0^{VDD} C_L dV_O - \int_0^{VDD} C_L \cdot V_O dV_O$$

$$= \frac{C_L}{2} VDD^2$$

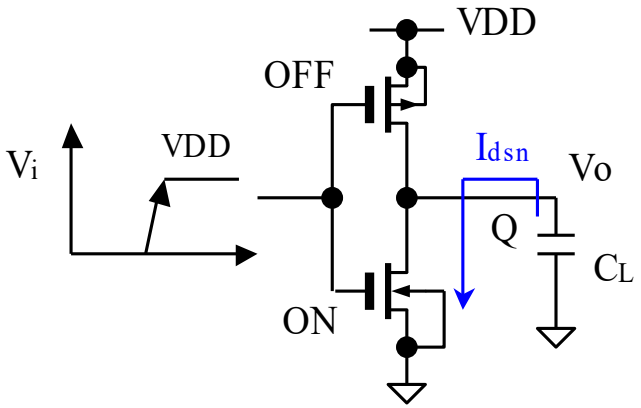
[Note] The total supply energy is $C_L VDD^2$. The half of them is dissipated from p-ch MOSFET and The half of them is storied in C_L.

Charge-discharge current (Discharge)

Discharge current and output voltage

$$Q = C_L \cdot V_O$$

$$I_{dsn} = -\frac{dQ}{dt} = -C_L \cdot \frac{dV_O}{dt}$$

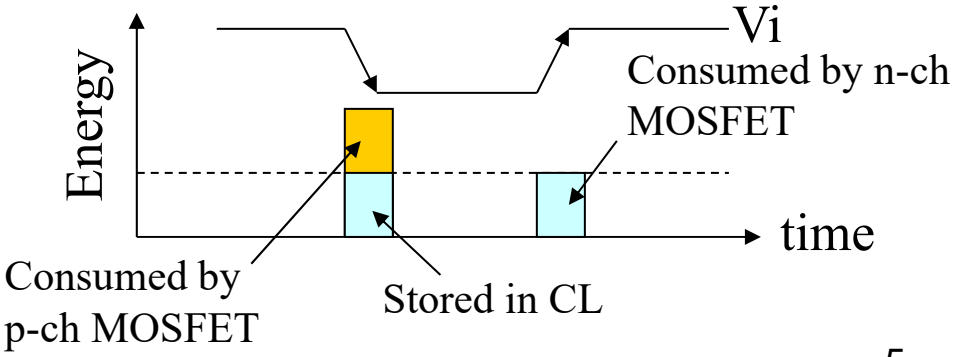


Energy consumption by n-ch MOSFET

$$E_d = \int_0^{\infty} I_{dsn}(t) \cdot V_O(t) dt$$

$$= \int_{VDD}^{0} (-C_L \cdot V_O) dV_O$$

$$= \frac{C_L}{2} VDD^2$$



Power consumption by charge-discharge current

Energy consumption of an inverter for a clock cycle

$$E_{cyc} = E_c + E_d$$
$$= C_L \cdot VDD^2 \quad \text{(J)}$$

An average power consumption P_{cd} for a clock cycle

$$P_{cd} = E_{cyc} / T_C$$
$$= C_L \cdot f_C \cdot VDD^2$$

2 transitions per 1 cycle

Important!

Clock frequency

Power supply voltage

⇦ Parameters to reduce the power consumption

Switching activity of a logic gate

D#srz hu#frqvxp swlrq#ri#jdwhv#ghshqgv#rq#wkh#wudqvlwlrq#suredelolw|#
ehwz hhq#wkh#rjlf#ydoxh1

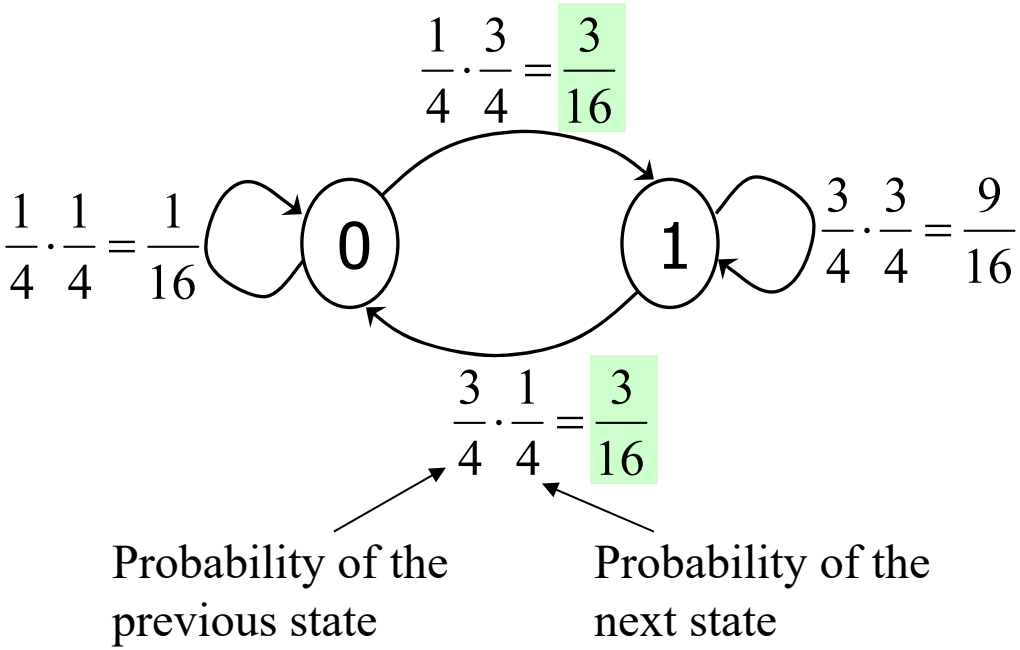
Example of 2-input NAND

A	B	Z	
0	0	1	Probability 3/4
0	1	1	
1	0	1	
1	1	0	Probability 1/4

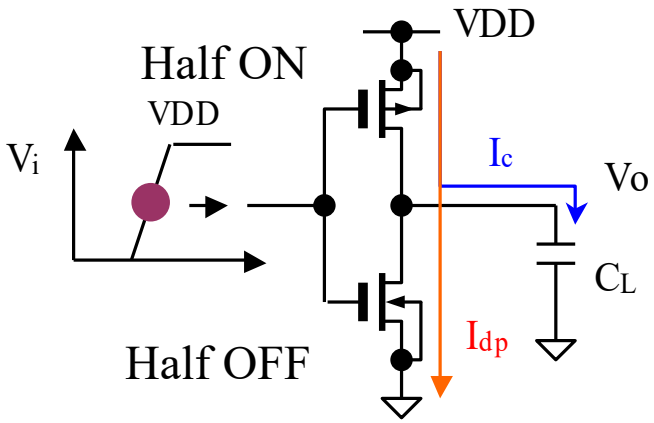
$$P_{cd} = C_L \cdot VDD^2 \cdot \frac{6}{16} f_C$$

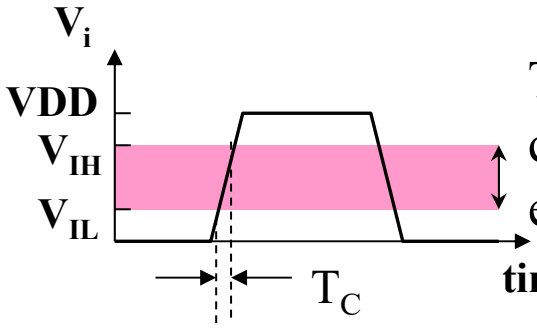
Energy consumption for 1 cycle

Transition probability $P_{0\Leftrightarrow 1}$=6/16



Direct path short circuit current





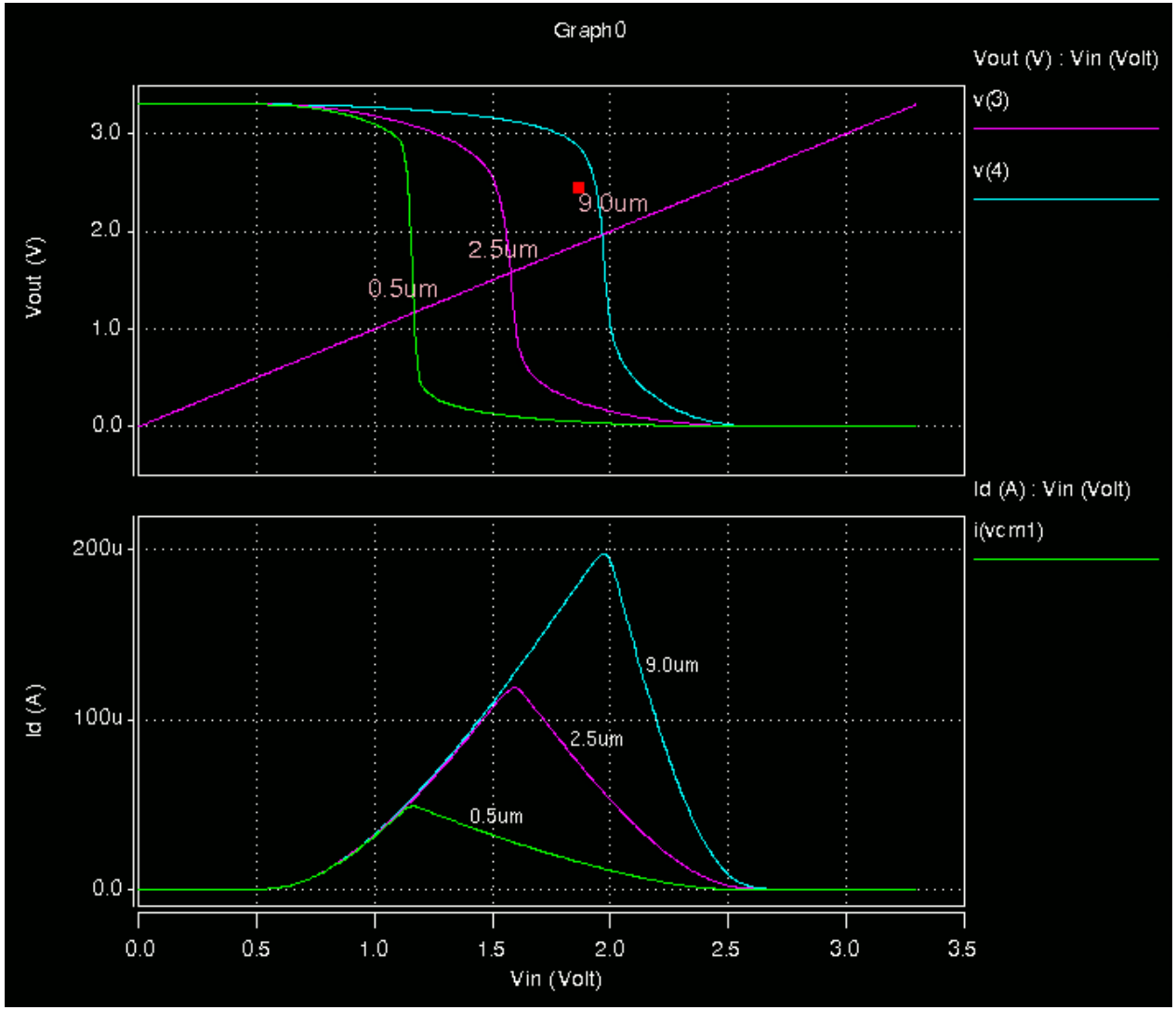
The both p-ch and n-ch MOSFETs are electrically conducted.

$$P_{dp} = VDD \cdot f_C \cdot 2\int_0^{T_C} I_{dp}(t) \cdot dt$$

$$\cong 2 \cdot VDD \cdot f_C \cdot \overline{I_{dp}} \cdot T_C$$

1. The current in p-ch MOSFET is branched to the short circuit current I_{dp} and the charge-discharge current I_c. If the current I_c is large enough, the current I_{dp} is ignored.
2. The short rise time and fall time of input signal are effective to reduce the current P_{dp}.

Maximum direct path short circuit current

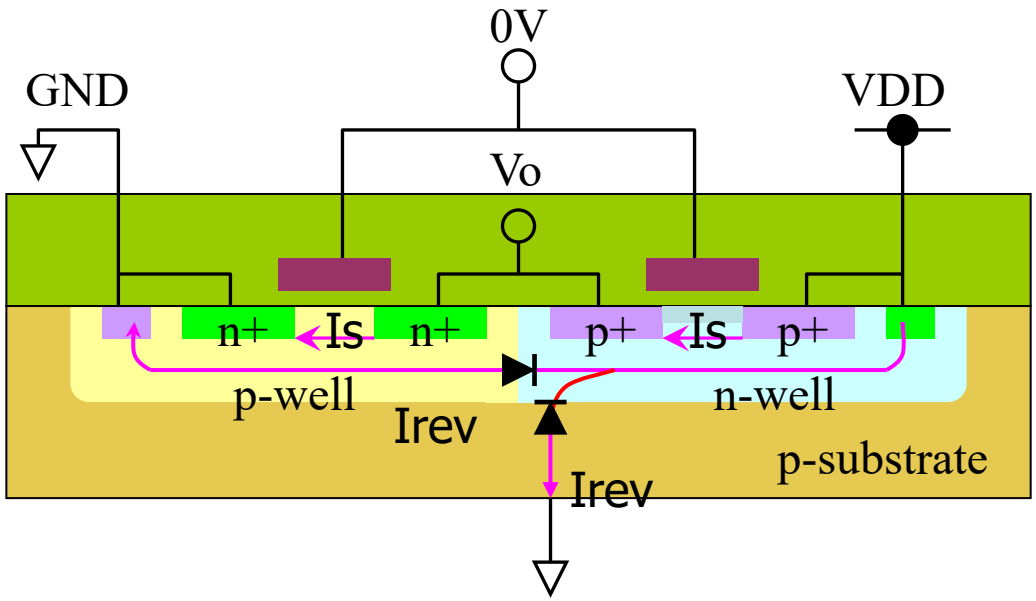


DC transfer characteristics. W_n = const. and W_p is a parameter.

The maximum current and gate threshold depend on W_n and W_p, respectively.

Leakage currents

A leakage currents is increasing with shrinking the MOSFET size.



- Reverse current of pn junctions I_{rev}
- Subthreshold current of MOSFET Is
- Gate tunneling current I_T

The leakage current increases with shrinking the size of MOSFETs.

$$P_l = VDD \cdot I_{leak}$$
$$= VDD \cdot (I_{rev} + I_S + I_T)$$

Estimation of power consumption

The total power consumption P_{total} is the sum of the dynamic power consumption P_{at} and the static power consumption P_{st}. The power consumption by the direct path short circuit current can be typically ignored.

$$P_{total} = P_{at} + P_{st}$$

$$\begin{cases} P_{at} \cong \kappa \cdot N_g \cdot P_{cd} = \kappa \cdot N_g \cdot f_C \cdot C_L \cdot VDD^2 \\ P_{st} \cong N_g \cdot P_l = N_g \cdot I_l \cdot VDD \end{cases}$$

N_g *Number of gates*
κ *Activity factor of gates*
C_L *Load capacitance per gate*
f_c *Clock frequency*

$$f_{max} = \frac{VDD}{3.70C_L}\frac{\beta_n\beta_p}{\beta_n + \beta_p}$$

P_{cd}	Power consumption by the charge-discharge current in a gate
P_l	Power consumption by the average leakage current in a gate
k	Transition probability of gate in a clock cycle

Low power design 1

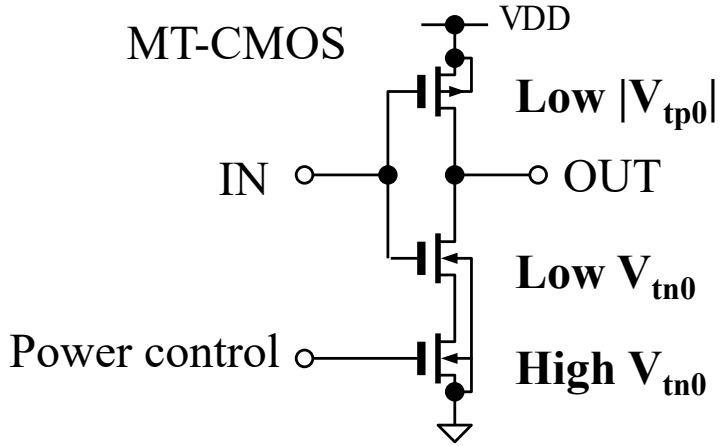
Reduction of P_{at}

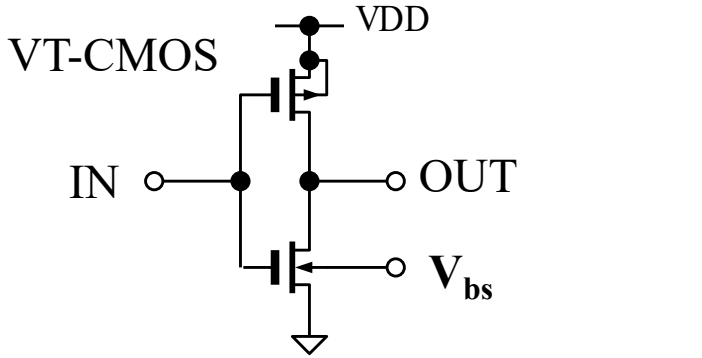
- Reducing the supply voltage VDD
- Reducing the clock frequency
- Clock gating for the circuit block in standby mode
- Reducing the operation amount (by the improvement of the algorithm)
- Implementation by asynchronous circuit without a clock signal
- Implementation by adiabatic logic circuit

Low power design 2

Reduction of P_{st}

- Reducing the supply voltage VDD
- Controlling the threshold voltage of MOSFET
  - MTCMOS (Multi-threshold CMOS)
    - Power gating by the high threshold MOSFET
  - VTCMOS (Variable threshold CMOS)
    - Leakage current reduction by controlling V_{bs}
  - Nonvolatile memory and power gating



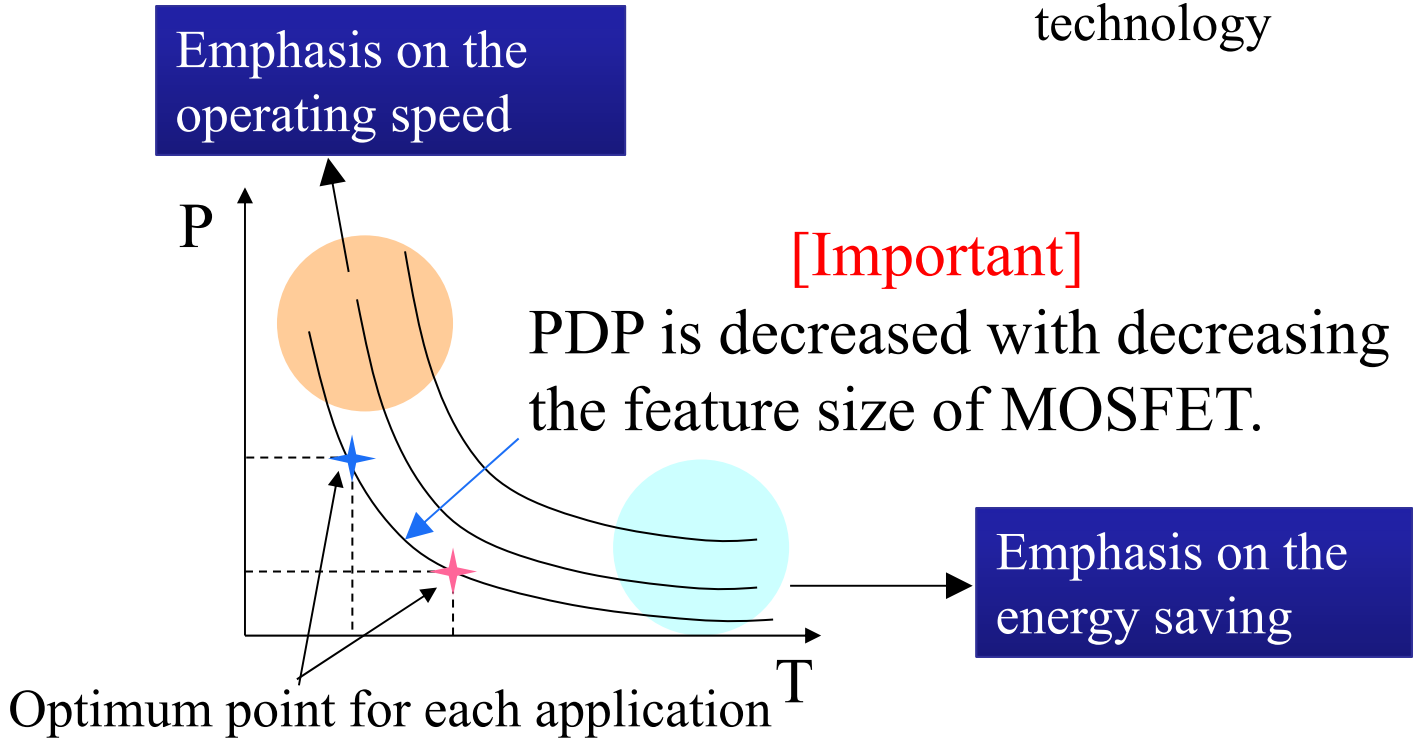


Operating mode $V_{sub}=0$
Standby mode $V_{sub}<0$

Power-delay product (PDP)

For an inverter, $PDP = P_{at} \cdot t_d = C_L f_c VDD^2 \frac{1}{f_c}$

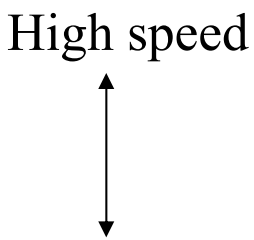
$= C_L VDD^2$ ⟵ Depends on the fabrication technology

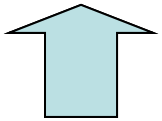


Packaging and power consumption

Allowable power loss

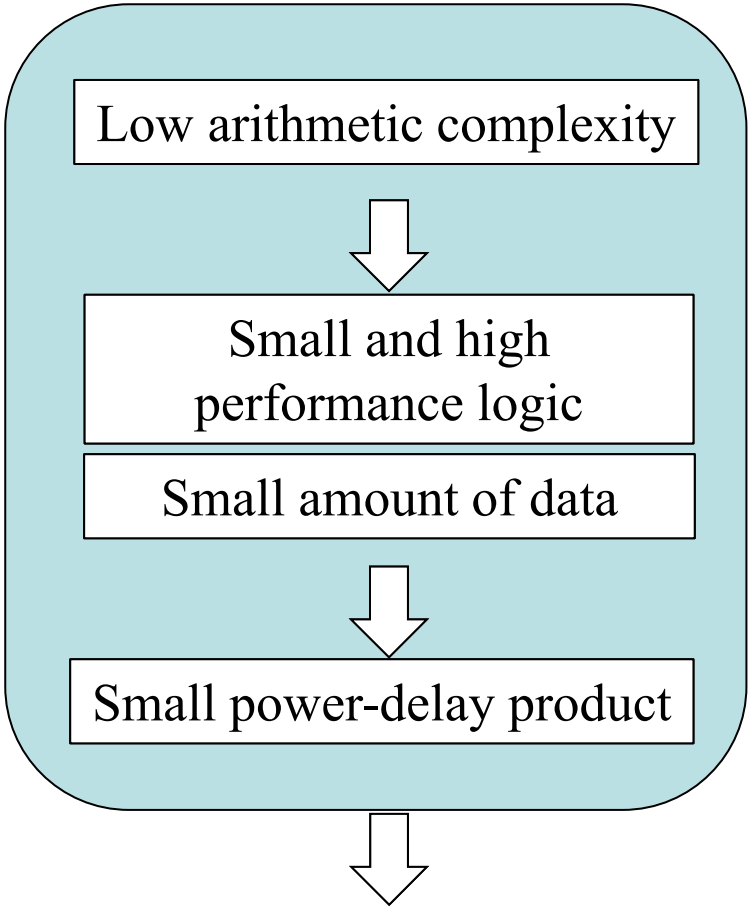
Ceramic package	10W
Plastic molding	1W
Mobile applications	0.1~0.01W
Energy harvesting	0.001W





Minimum clock frequency and Minimum power supply by the optimization of the operating point on PDP curve.

System optimization of digital LSI



High performance system

← Evaluation in algorithm design

← Evaluation in logic design

← Evaluation in logic design

← Technology options to optimize the PDP

[Note] A top-down design method with CAD software and emulator is effective to optimize the whole system.