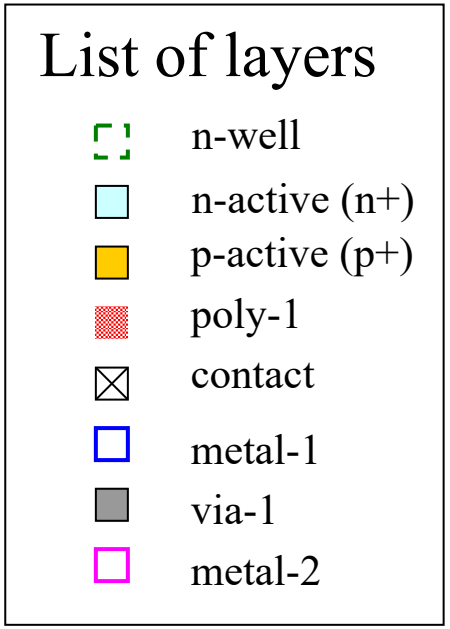
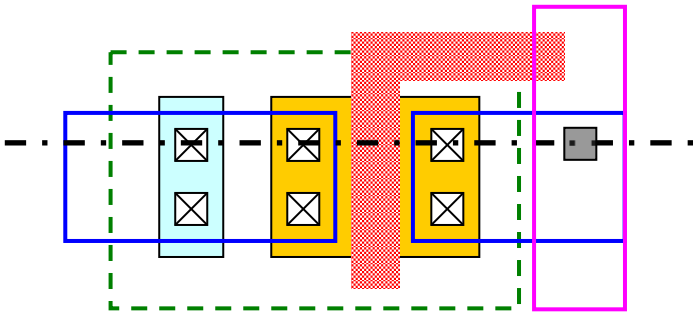
5.2 Layout design

Design flow of full custom LSI

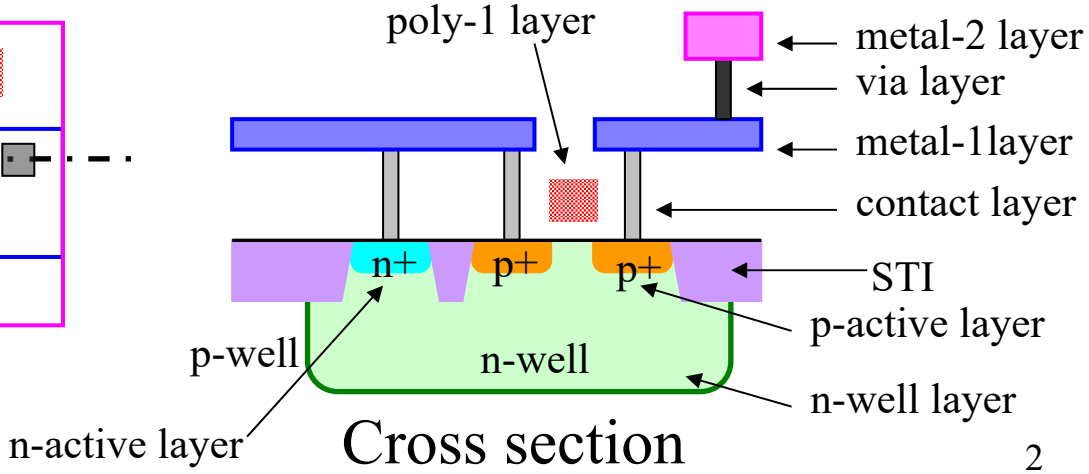
Layers

- The parts of the structure of the cross section, e.g. Metal, n-active, p-active, Poly silicon, correspond to the layers of the layout.
- The layout pattern is edited by a layout editor, which is a CAD software to draw the shapes on each layer and overlay them.





Top



Cross section

Design rules

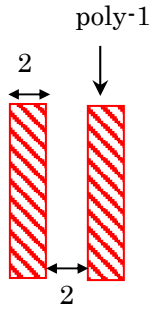
- The designers cannot specify the dimensions of the height in cross-section structure but design the layered structure by drawing the layout pattern.
- All layout patterns must comply with the design rules which is specified by the manufacture.
  - Accuracy assurance for photomask pattern
  - Accuracy assurance for microfabrication
  - Accuracy assurance for the variance of electrical characteristics
  - Preventing malfunctions due to the parasitic devices, e.g. parasitic pnp and npn (*).

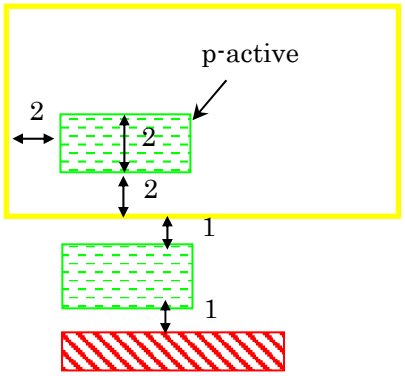
* The adjacent pn junctions operates as a bipolar junction transistor. Unintentional short between VDD and GND may occurs (latch-up phenomenon).

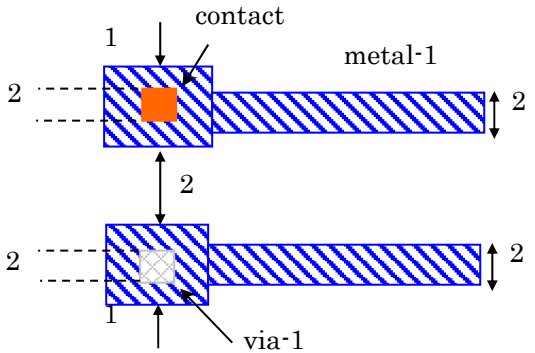
Layout verification

- Violation of design rules can be automatically detected by DRC (Design Rule Check) software.
  - A design data that violate a design rule is not accepted by manufacture.
- Scalable rule (Lambda rule) and micron rules
  - In the l rules, all rules are defined as a function of a parameter λ. The feature size of the process sets to be 2 λ. The portability between technologies is enhanced by lambda rules.
  - In the μ rules, all rules are defined in absolute dimensions. The μ rule is adopted in advanced process technologies.
- Verifications of layout design
  - **DRC (Design Rule Check)** Design rule violation
  - **ERC (Electrical Rule Check)** Detection of open and short error
  - **LVS (Layout VS Schematic)** Equivalence between layout and schematic

Example of design rules







poly-1 rules

Width > 2

Spacing > 2

active rules

Width > 2

Spacing from well edge > 2
(Inside the well)

Spacing from well edge >1
(Outside the well)

Spacing from poly-1 > 1

metal-1 rules

Width > 2

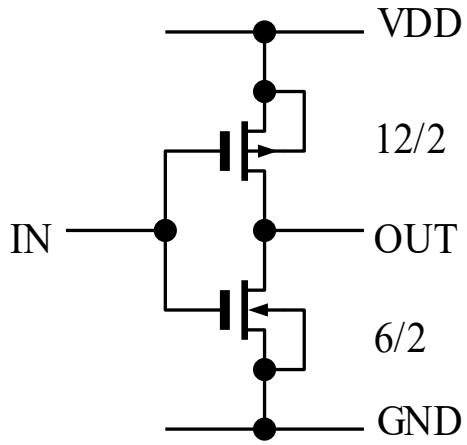
Spacing > 2

Overlap with contact > 1

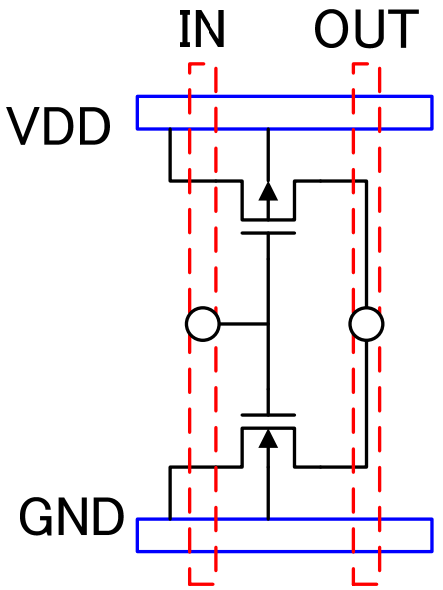
Overlap with via-1 > 1

Layout design flow of inverter 1

1. Place the MOSFETs so that the wires are wire orthogonal to each other.



Schematic

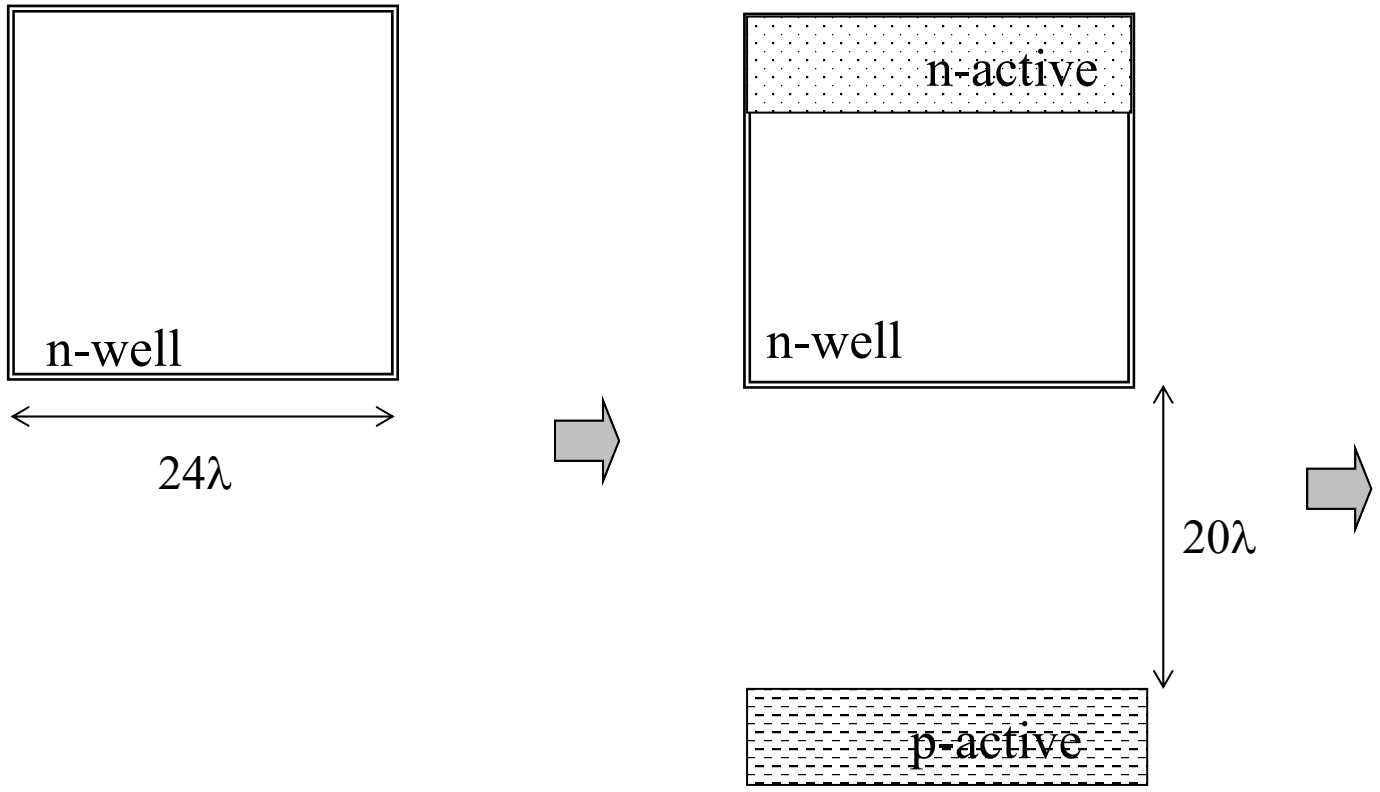


Stick diagram
(modified to design a layout)

The numbers attached to the MOSFETs (e.g. 12/2, 6/2) show the values of W/L.

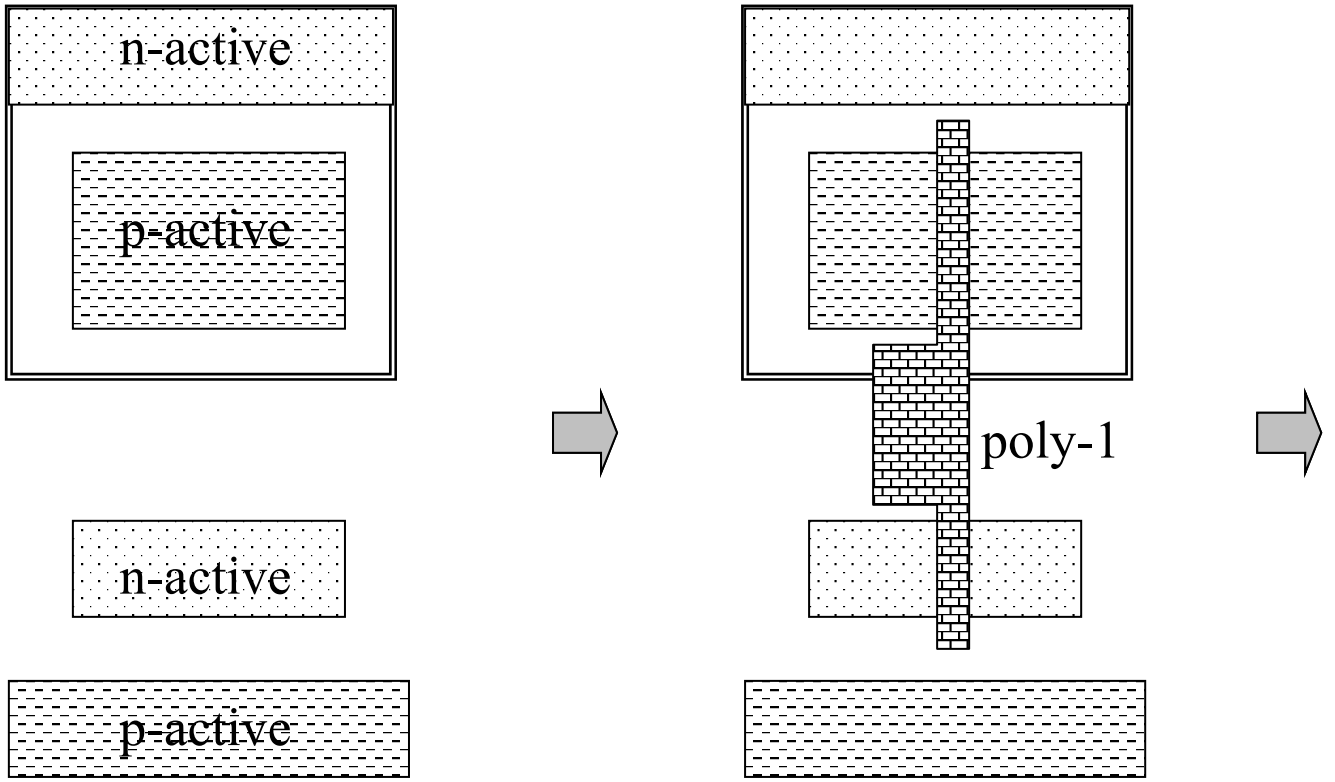
Layout design flow of inverter 2

2. Put the n-well area.
3. Put the n-active area for the n-well contact and the p-active area for the p-substrate contact.



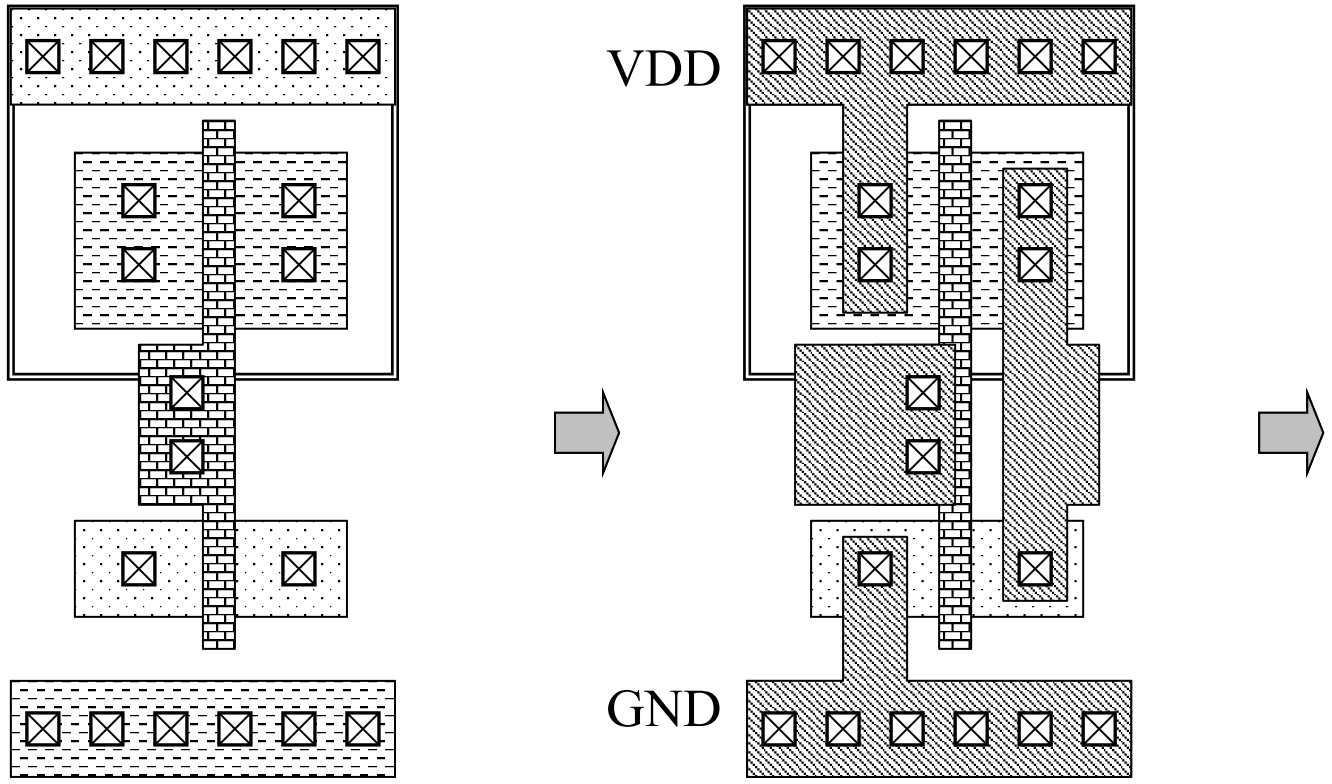
Layout design flow of inverter 3

4. Draw the n-active area and the p-active area to define the source and drain of MOSFETs.
5. Put the poly-1 (Gate) electrode to separate the source and drain.



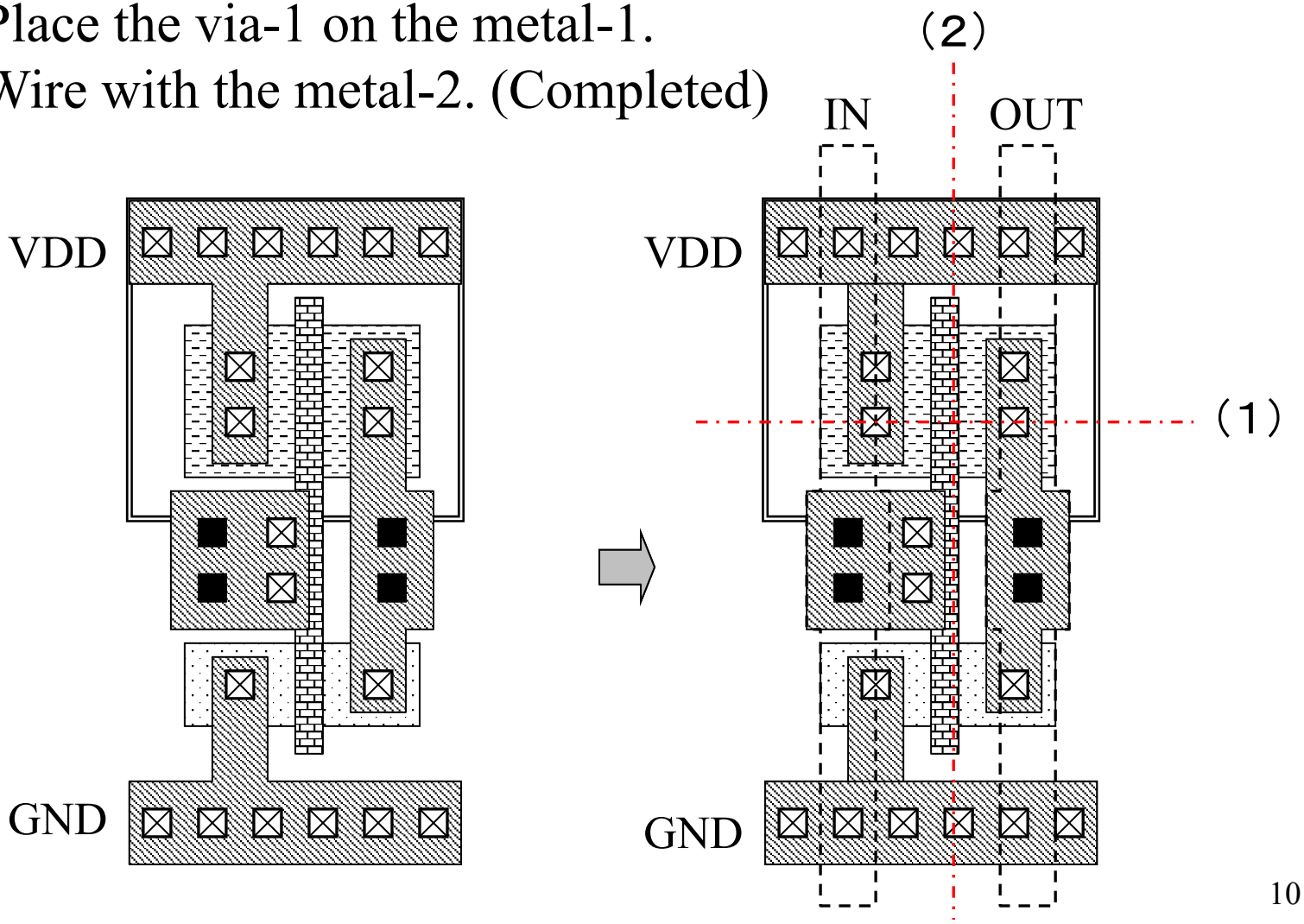
Layout design flow of inverter 4

6. Put the contacts on the p-type and n-type active areas.
7. Wire with the metal-1.

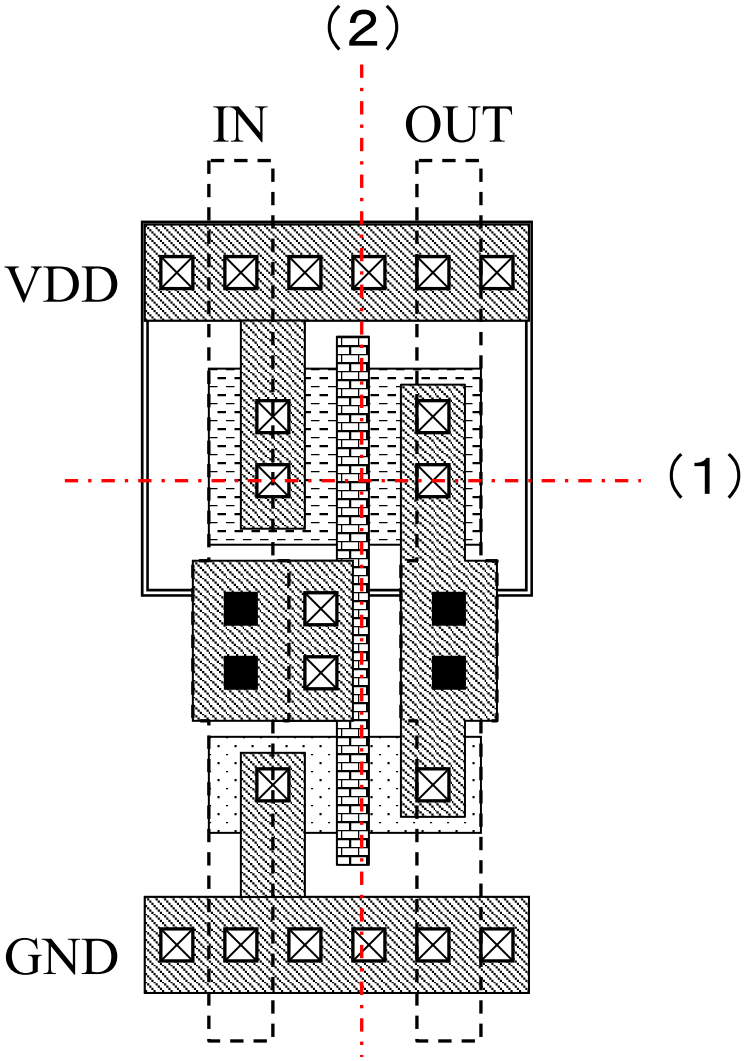


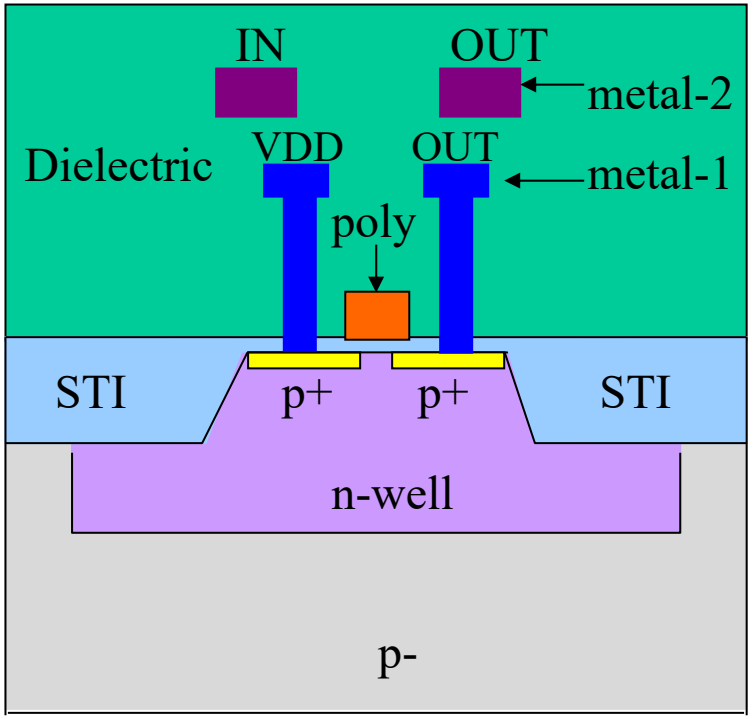
Layout design flow of inverter 5

8. Place the via-1 on the metal-1.
9. Wire with the metal-2. (Completed)



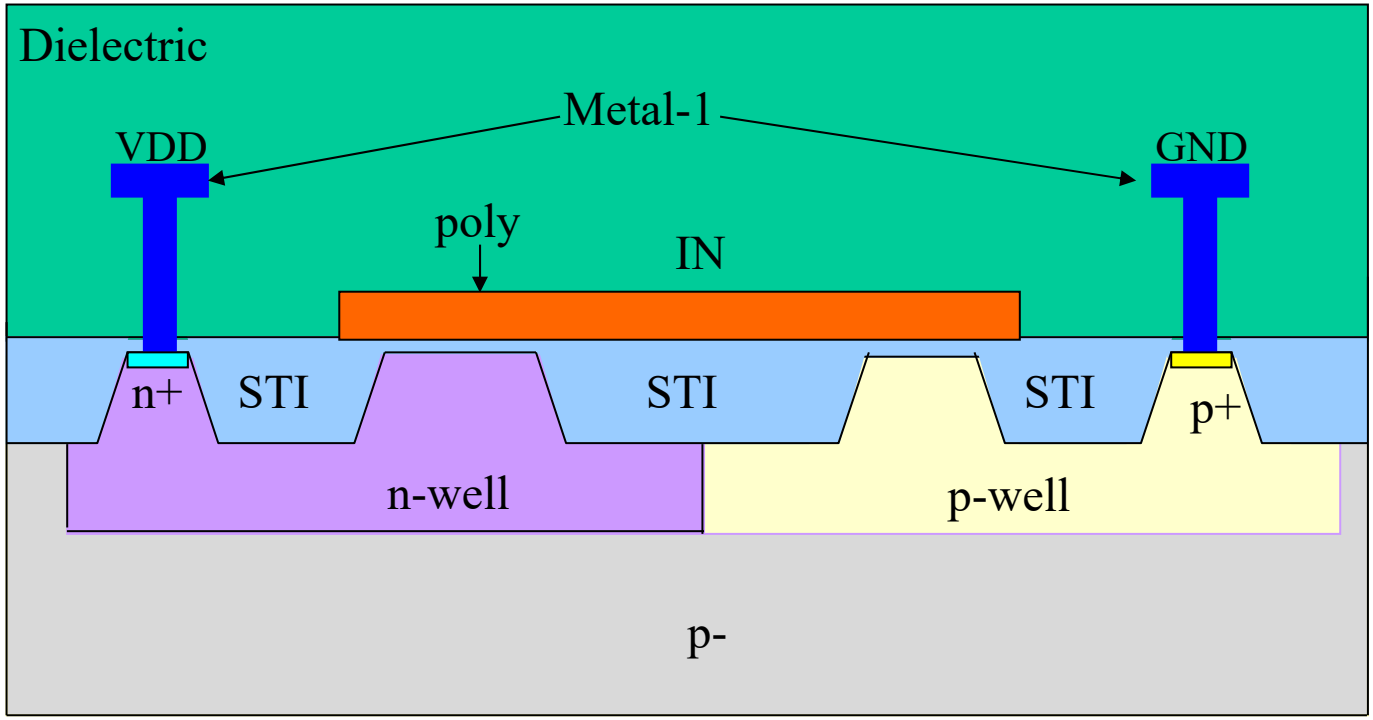
Cross section of inverter 1





Cross sectional view along Line (1)

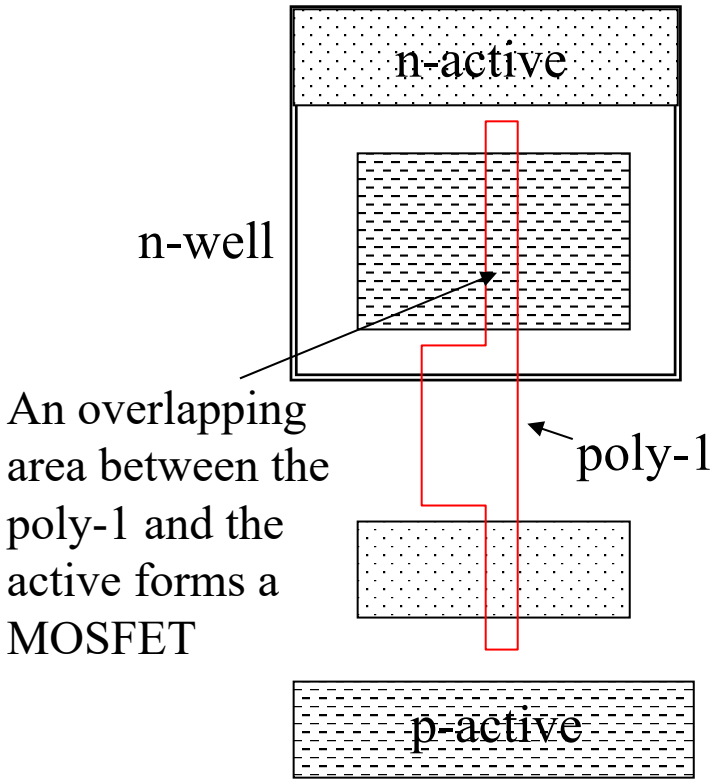
Cross section of inverter 2



Cross sectional view along Line (2)

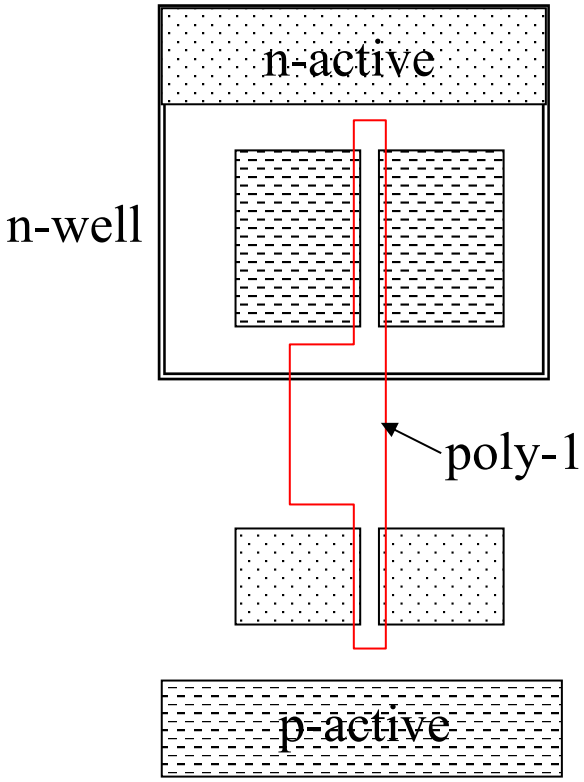
[Important note] layout of MOSFET

○



Correct

×

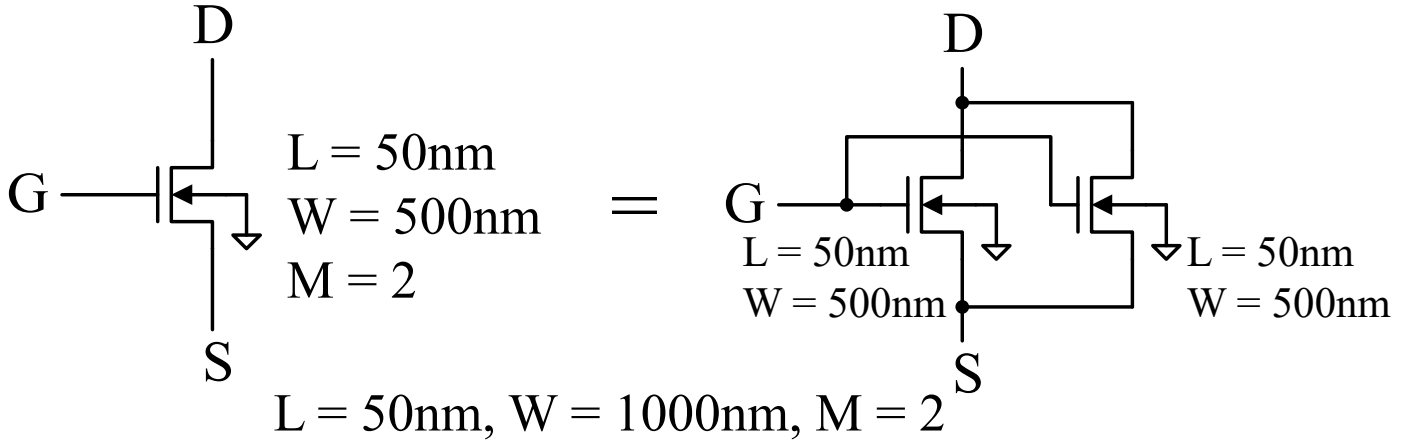


Incorrect

If you draw the source and drain as two closed regions,
the MOSFET is not formed but the gate electrode is formed on the FOX.

Fingers of MOSFET

- W/L ≦ 20 (Typically, W/L = 2~10)
  - The circuit performance is degraded with increasing W of MOSFET, because the large W causes the large parasitic resistance in the gate electrode. The value of W/L should be set within the range of 20.
- W/L > 20, The parameter M (Multiplier) equivalently increase the value of W/L.
  - M-parameter is defined as number of parallel connections.
  - The large W is required to flow the large current.

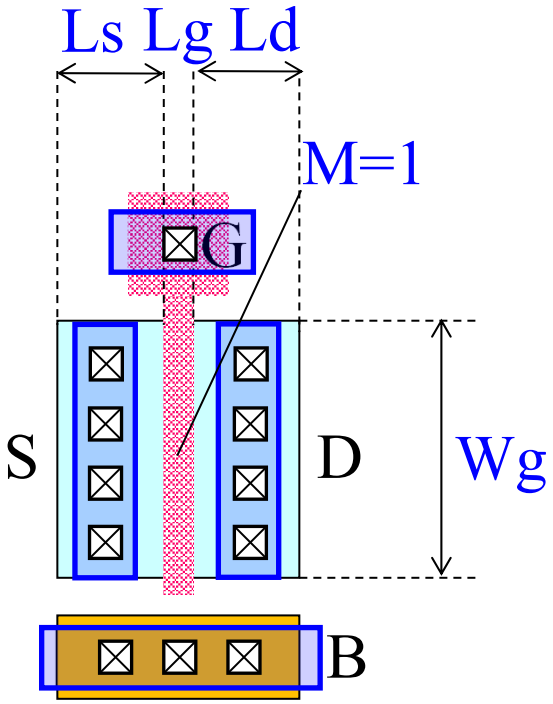


[Note] Design parameters of MOSFET

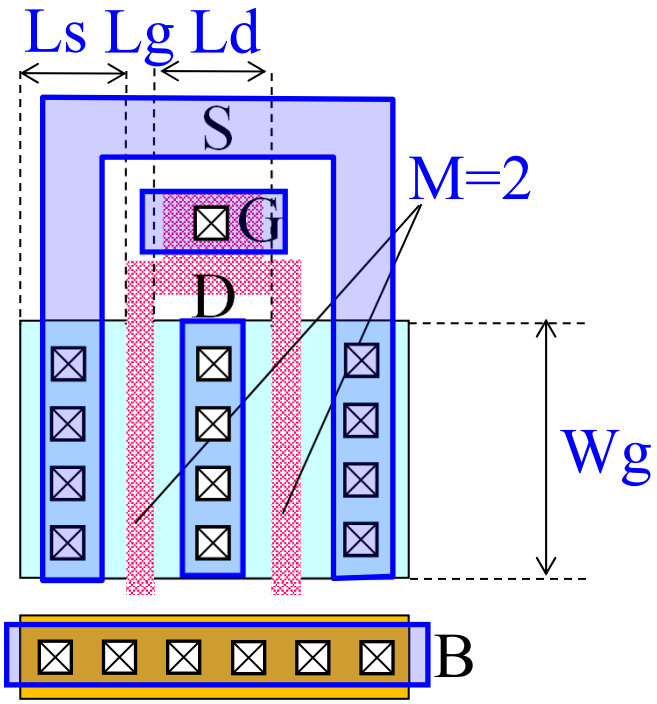
n-active (n+)　p-active (p+)　poly-Si　contact

SPICE Parameter	Value
L	Lg
W	Wg
AD	Wg･Ld
AS	Wg･Ls
PD	Wg+2Ld
PS	Wg+2Ls
M	並列接続数

For example of M=2,
AD = Wg･Ld/2
PD = Wg + Ld

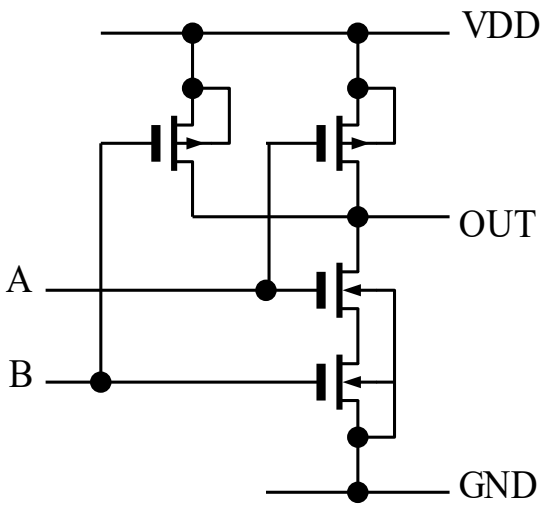


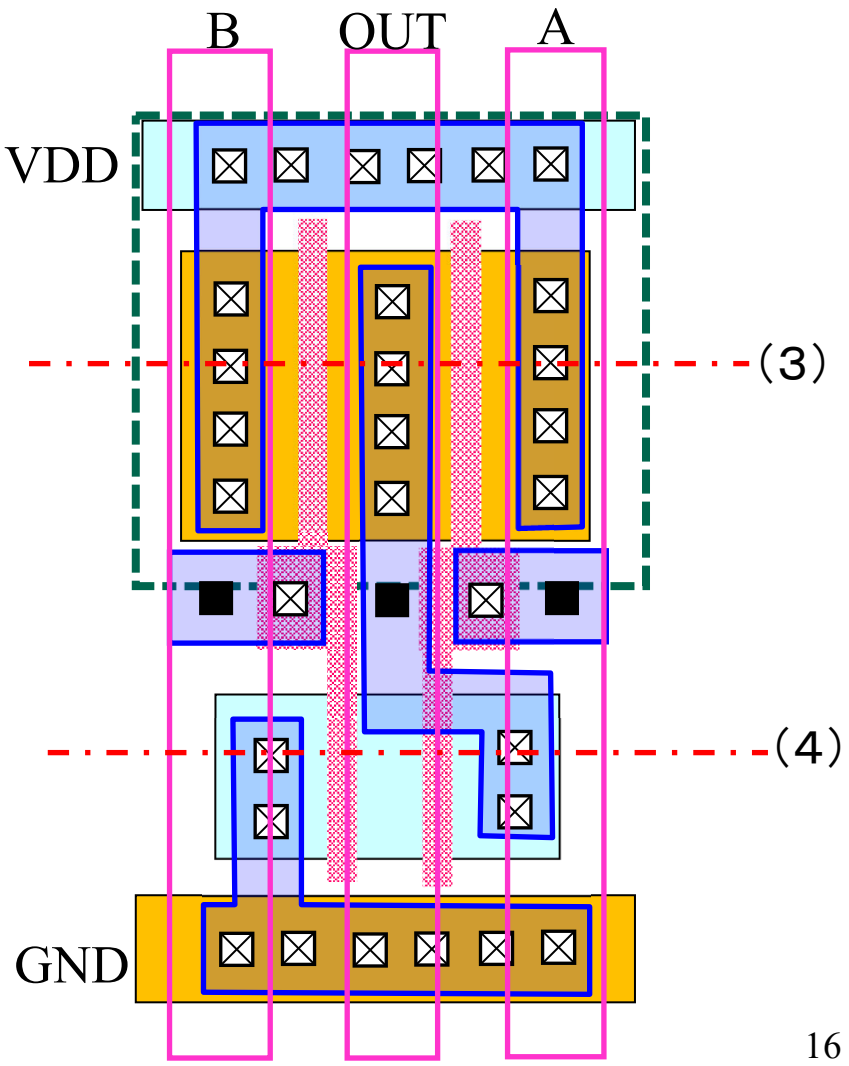
n-ch MOSFET (M=1)



n-ch MOSFET (M=2)

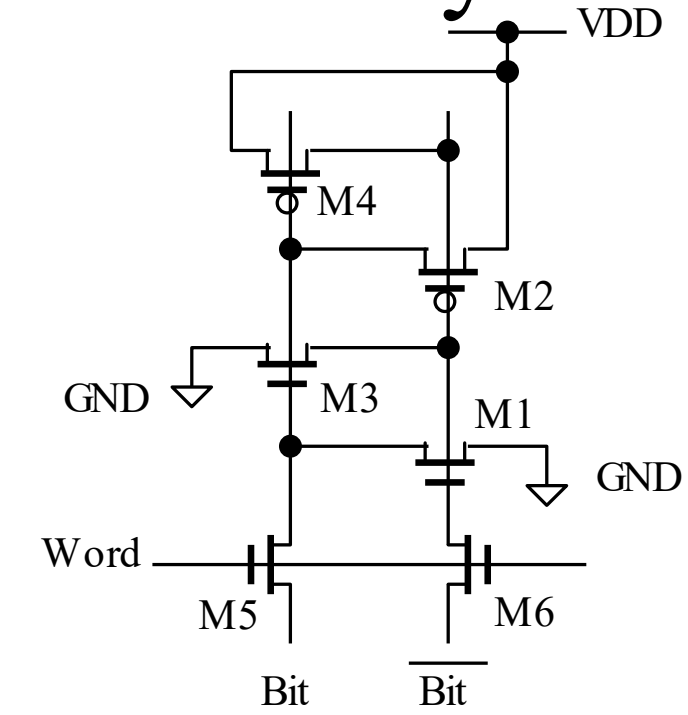
Layout of NAND

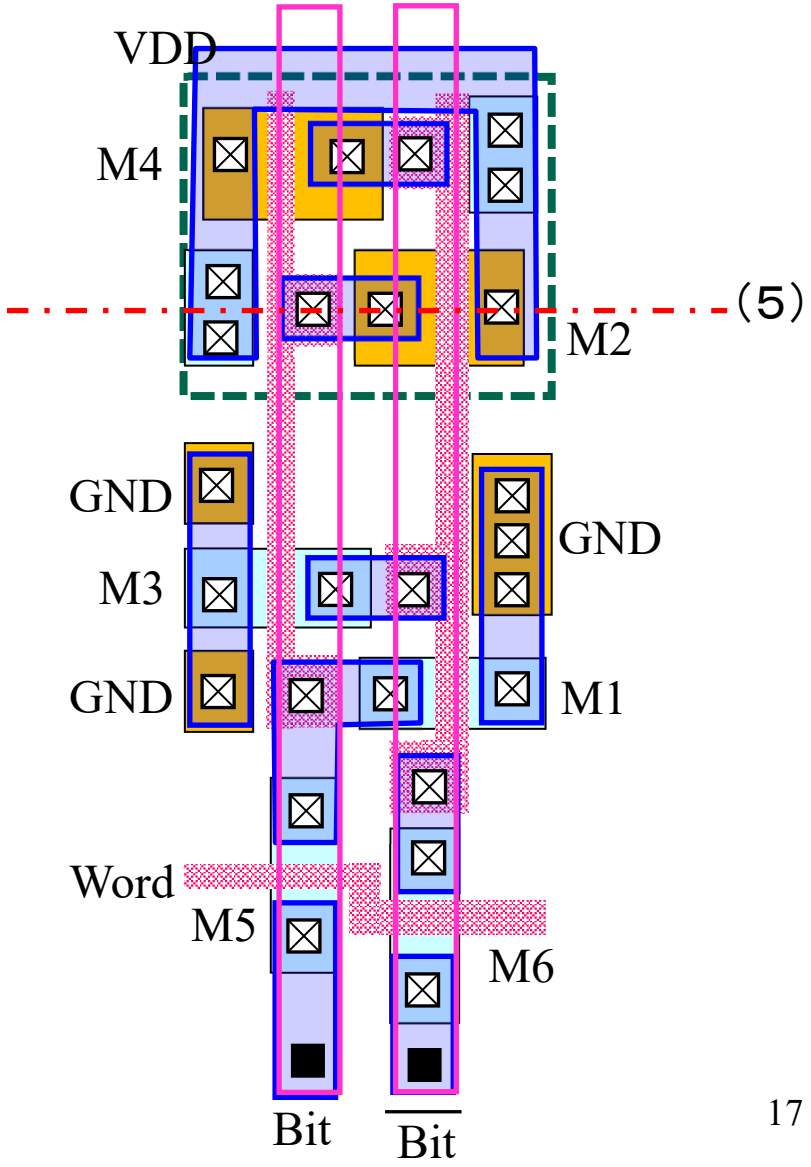




n-well
n-active (n+)
p-active (p+)
poly-Si
contact
metal-1
via
metal-2

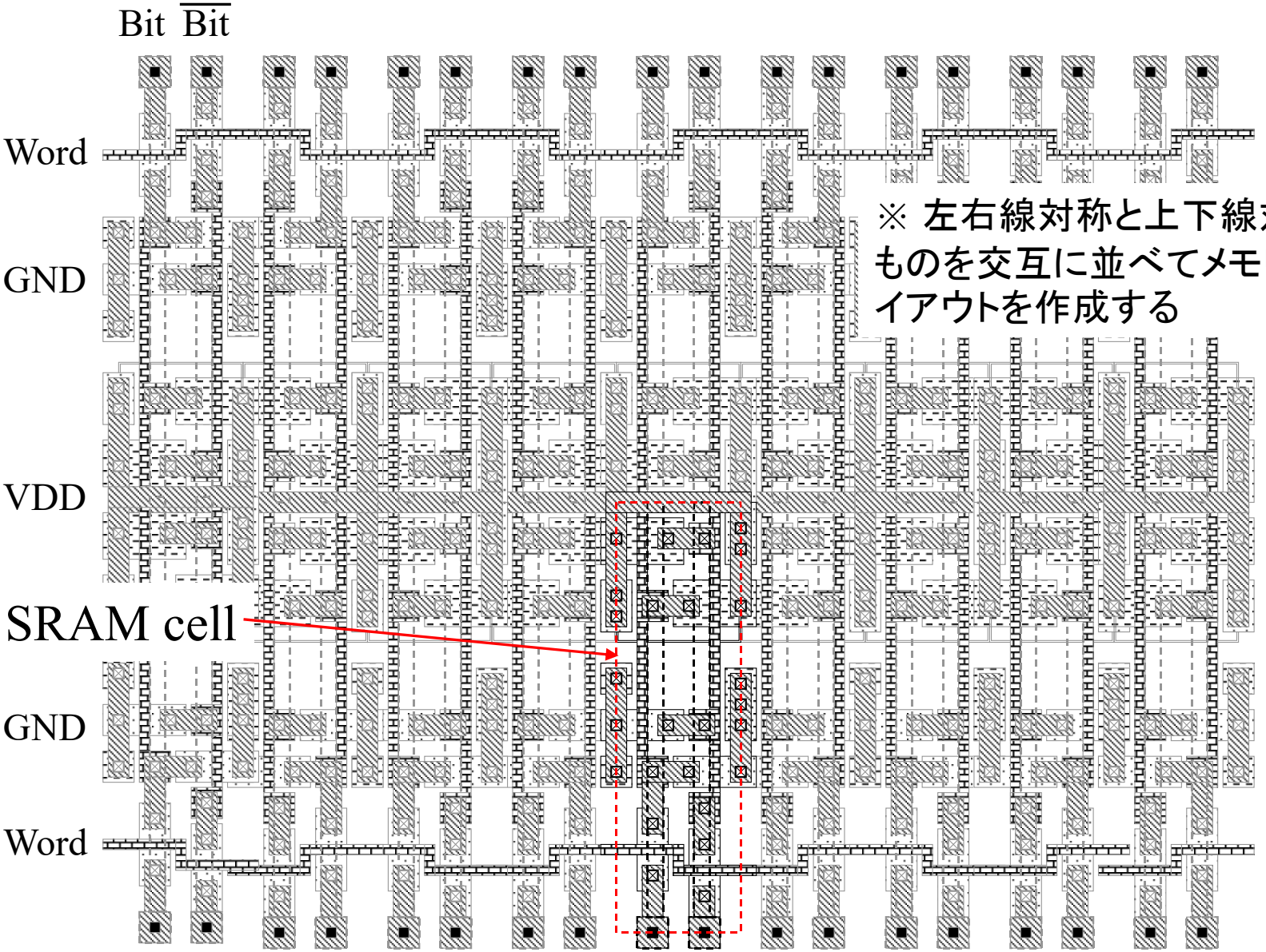
Layout of SRAM cell





n-well
n-active (n+)
p-active (p+)
poly-Si
contact
metal-1
via
metal-2

Layout of memory cell array



※ 左右線対称と上下線対称のものを交互に並べてメモリのレイアウトを作成する