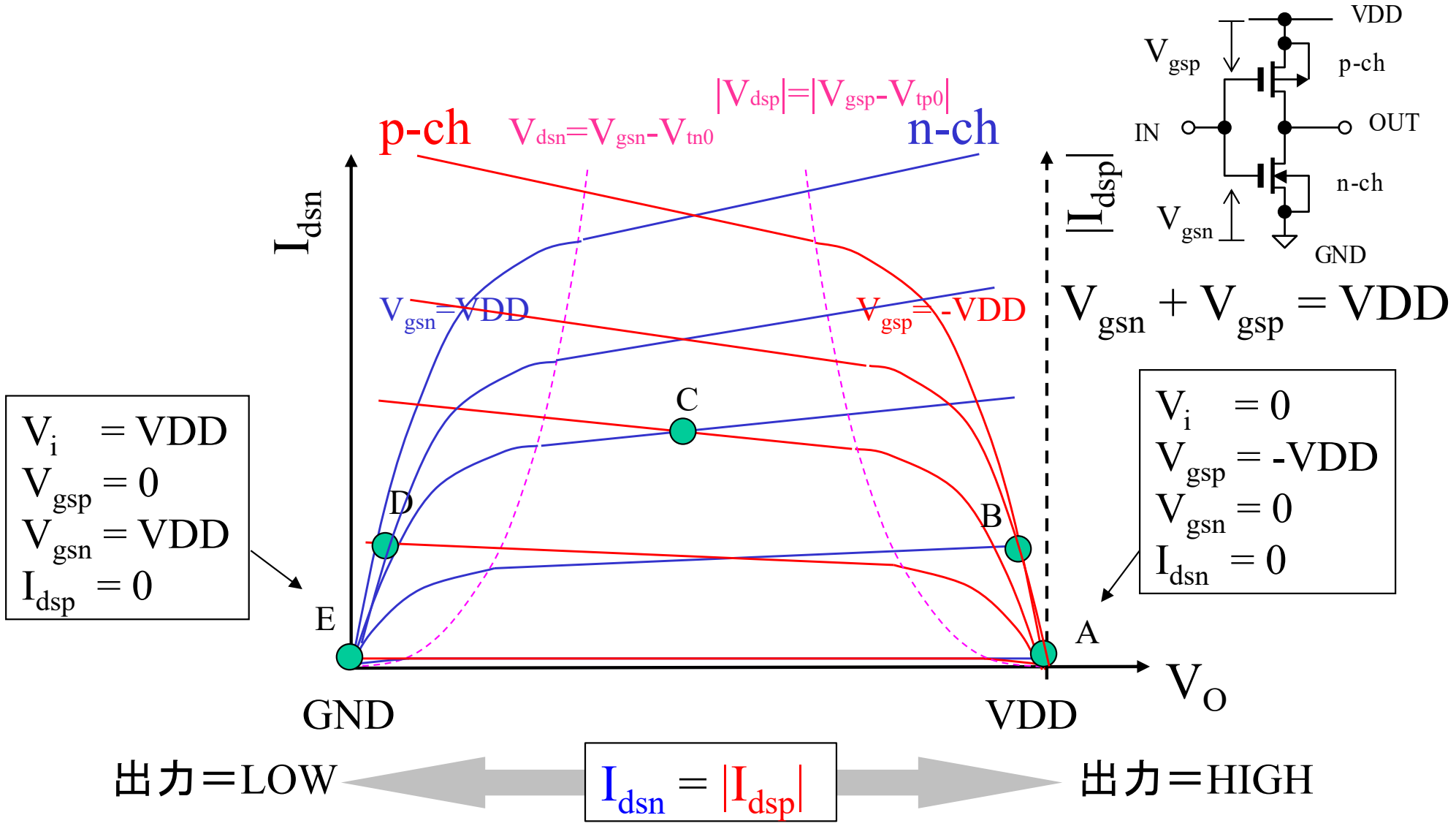
4.4 DC transfer characteristic

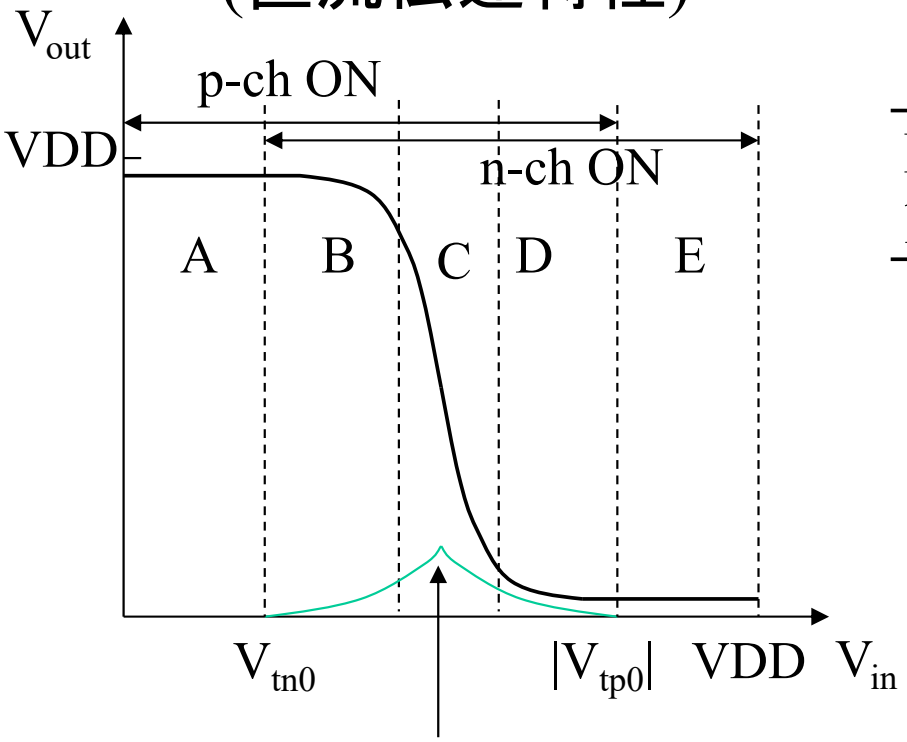
Noise margin and switching threshold voltage

Transient of the operating point



DC transfer characteristic

(直流伝達特性)



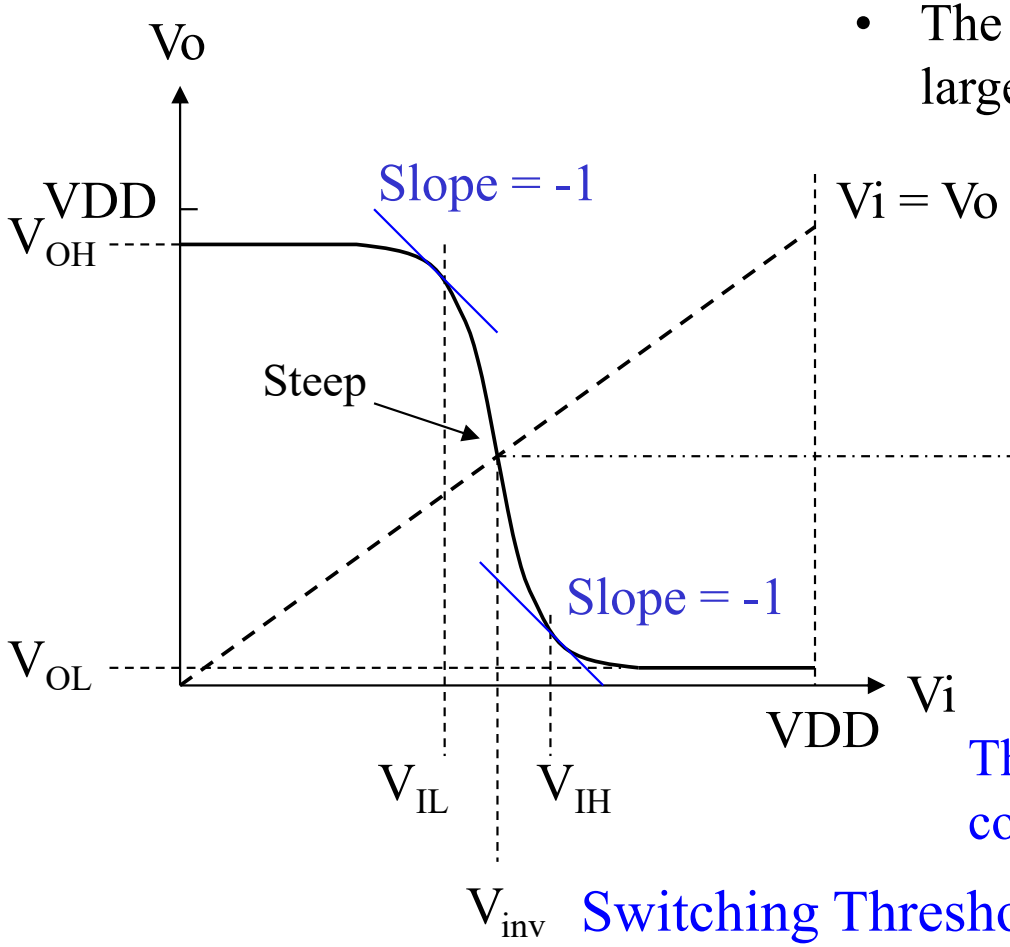
Input level	n-ch	p-ch
A	Sub-threshold	Linear
B	Saturation	Linear
C	Saturation	Saturation
D	Linear	Saturation
E	Linear	Sub-threshold

$I_{dsn} = -I_{dsp}$ (Through-current)

The current flows for a moment of rising or falling edge of the input signal.

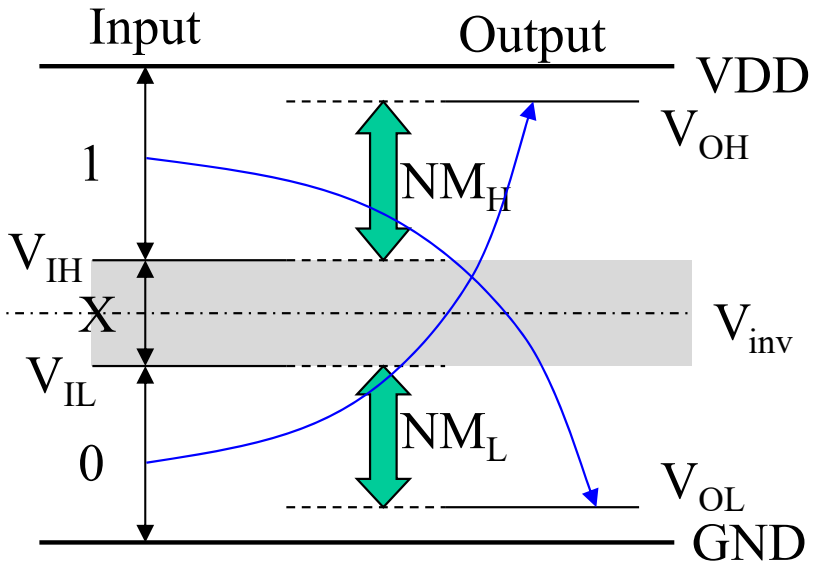
Noise margin

DC transfer characteristic



Noise margin (雑音余裕度) = NM_H, NM_L

- A large noise margin prevents errors.
- The noise margin of CMOS static logic is larger than that of other circuits.

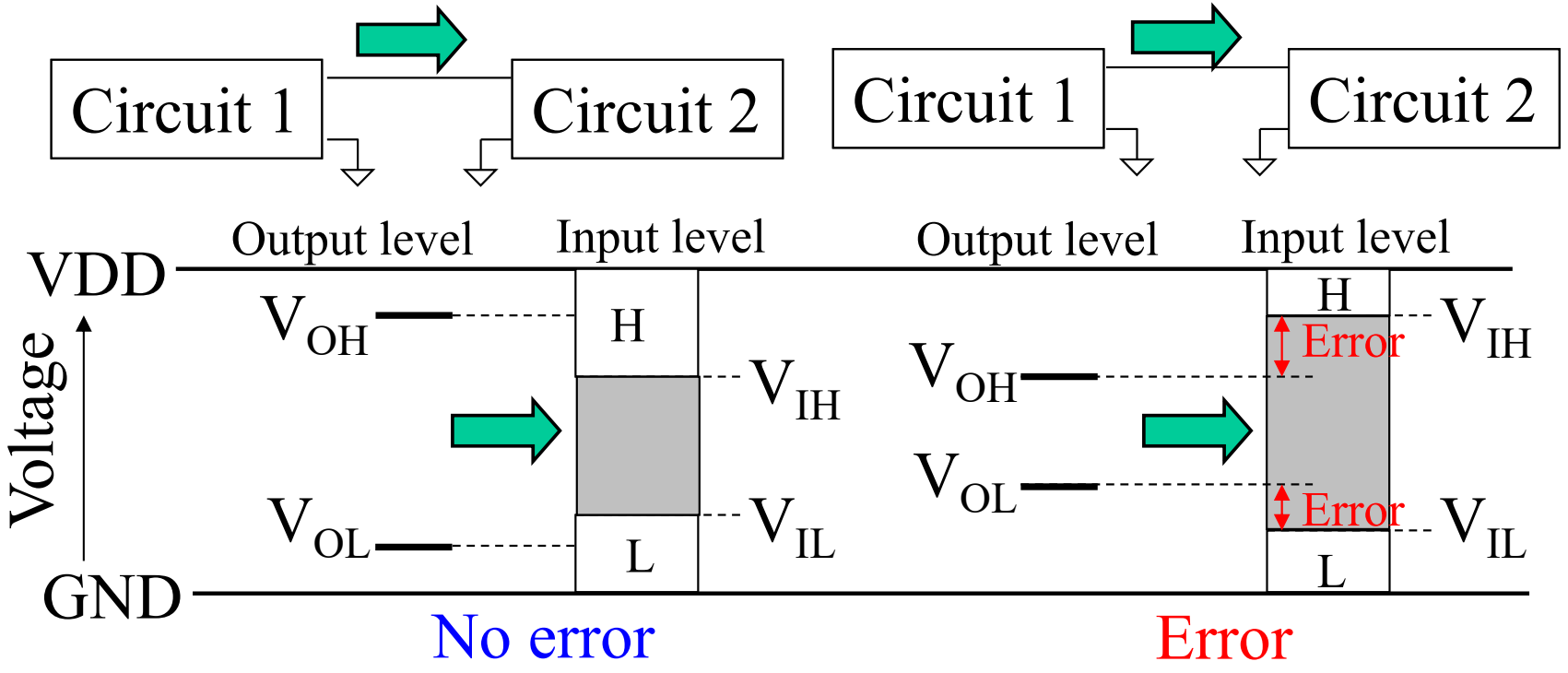


The amplitude error of the input voltage is corrected by the voltage gain of logic gates.

V_{inv} Switching Threshold Voltage
（ゲートのスイッチング閾値電圧）

Threshold level

- The values of V_{IH}, V_{IL}, V_{OH}, and V_{OL} are called threshold levels or IO levels.
- The threshold level depends the supply voltage and the circuit configuration. The circuits designed for the different threshold level cannot transfer the signals. (The level converter is required.)



IO level

- The standard threshold levels of IO circuits (IO level) are defined to transfer the signals between the commercial LSIs.
- The circuits with the different threshold level cannot be directly connected.
  - Level converter
  - Open drain
- The IO level of FPGA is programmable.

Standard IO level	V_{IL}(max)	V_{IH}(min)	V_{OL}(typ)	V_{OH}(typ)
CMOS(5V), LVCMOS(3.3, 2.5, 1.8, 1.5, 1.2V)	0.2*VDD	0.7*VDD	0.4V	VDD - 0.8V
TTL/LVTTL	0.8V	2.0V	0.35V	2.7V

TTL (Transistor-Transistor Logic): A type of bipolar transistor logic.

L_n, L_p, W_n, W_p, and V_{inv}

Gain coefficient βn, βp

$$\begin{cases} \beta_n = \dfrac{W_n}{L_n}\mu_n C_O \\ \beta_p = \dfrac{W_p}{L_p}\mu_p C_O \end{cases}$$

Usually, the manufacture controls the threshold voltage of MOSFET in order that $V_{tn0} = -V_{tp0} = V_T$.

$$I_{dsp} = -I_{dsn}$$

$$\frac{\beta_p}{2}(V_{inv} - VDD + V_T)^2 = \frac{\beta_n}{2}(V_{inv} - V_T)^2$$

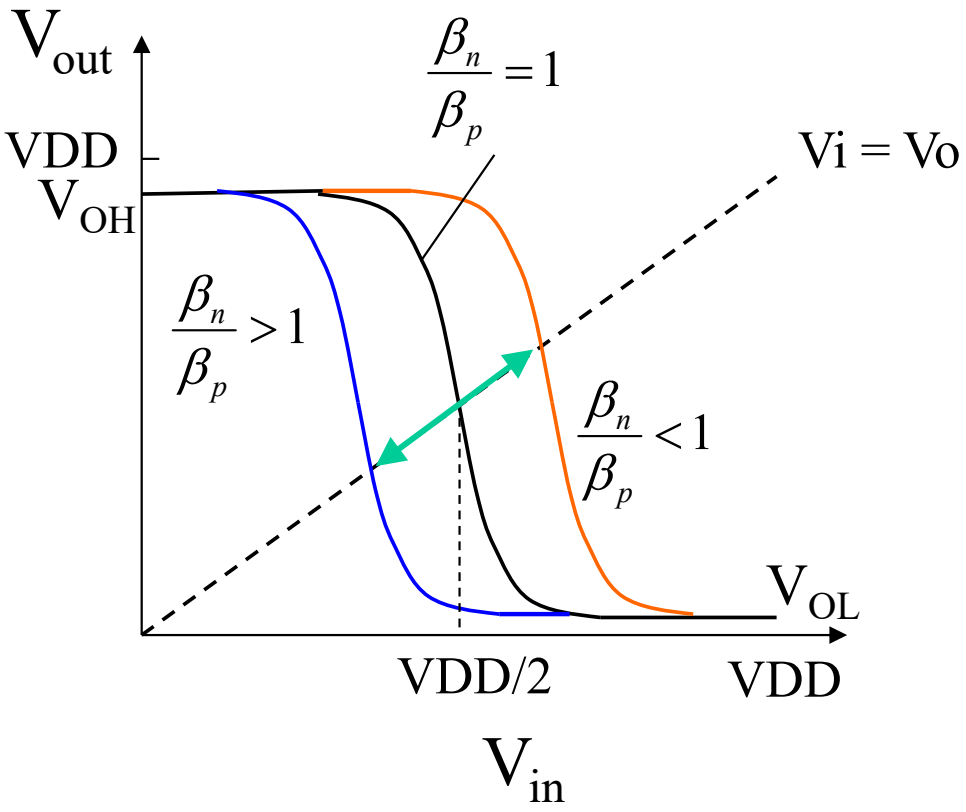
⇩

Switching threshold of inverter $V_{inv} = \dfrac{VDD - \left(1 \mp \sqrt{\dfrac{\beta_n}{\beta_p}}\right) V_T}{1 \pm \sqrt{\dfrac{\beta_n}{\beta_p}}}$

Design of gate switching threshold V_{inv}

From the previous slide, $\sqrt{\frac{\beta_n}{\beta_p}} = 1$

When $\beta_n = \beta_p$, $V_{inv} = \frac{VDD}{2}$



The output level V_{OH} and V_{OL} is fixed.

When V_{inv} = VDD/2, NM_H and NM_L become equivalent.

(The small noise margin causes errors.)

Optimization of L_n, L_p, W_n, W_p -1

$$\beta_n = \beta_p$$

$$\frac{W_n}{L_n}\mu_n C_O = \frac{W_p}{L_p}\mu_p C_O$$ ← The capacitance of gate oxide of n-ch MOSFET is exactly equals to that of p-ch MOSFET.

$$\boxed{\frac{W_n}{L_n}\mu_n = \frac{W_p}{L_p}\mu_p}$$

$$\frac{W_n}{L_n} : \frac{W_p}{L_p} = 1 : 1.5 \sim 3.0$$ ← The mobility μ_n and μ_p depends on manufacturing process.

Optimization of L_n, L_p, W_n, W_p -2

The gate length L_n and L_p is normally set to the minimum size of the technology, because the operation speed of MOSFET with smaller L_n, L_p is larger.

$$\frac{W_n}{L_n}\mu_n = \frac{W_p}{L_p}\mu_p$$

When $L_n = L_p$

$$\frac{W_p}{W_n} = \frac{\mu_n}{\mu_p} = 1.5 \sim 3.0$$

⇨

In the practical circuit design, simulate the logic circuit under the condition of $W_p/W_n = 2$, then adjust W_p/W_n in order that the switching threshold equals to VDD/2.

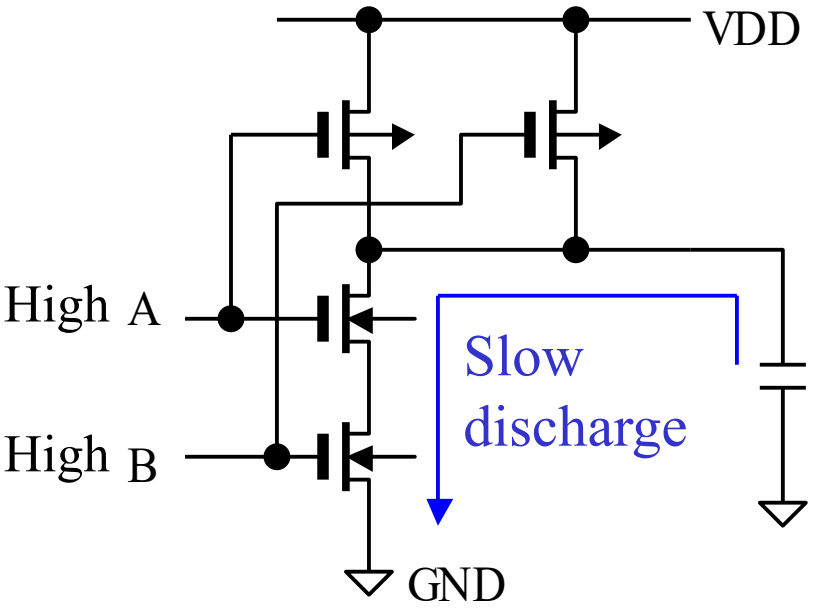
Waveform of output signal

Condition	V_{inv}	Speed of rising edge	Speed of falling edge	Output wave form
$\beta_n = \beta_p$	= VDD/2	Medium	Medium	
$\beta_n > \beta_p$	< VDD/2	Slow	Fast	
$\beta_n < \beta_p$	> VDD/2	Fast	Slow	

When $V_{inv} = VDD/2$, NM is maximized, and the rising speed and the falling speed is balanced.

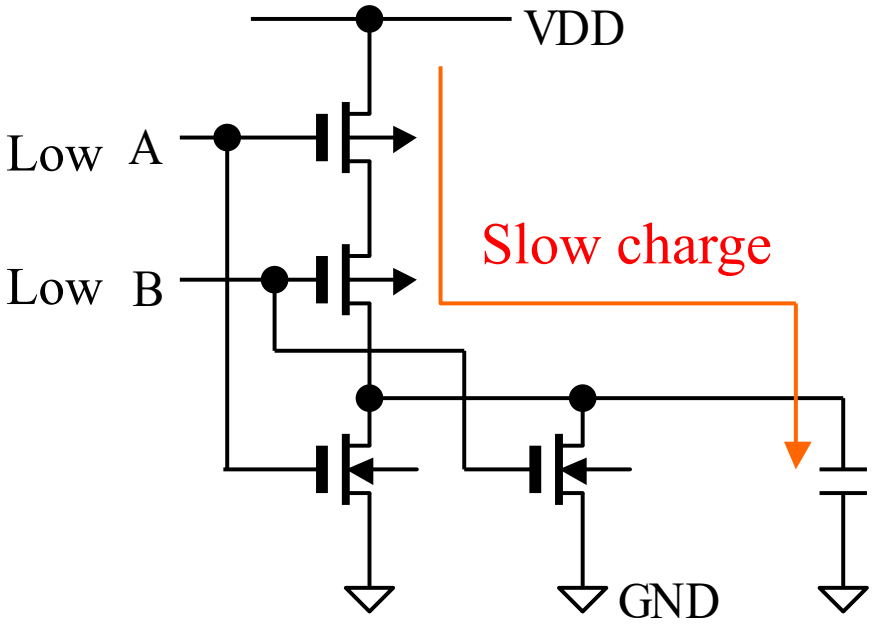
DC transfer characteristic of multi-input gates

NAND



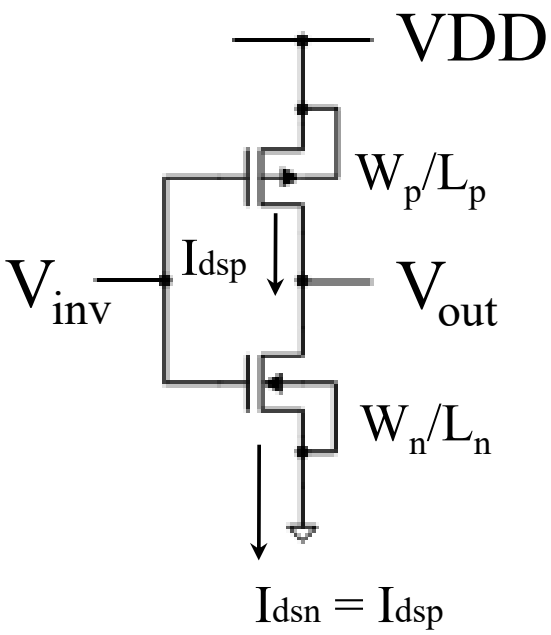
To improve the discharge speed, W_n must be larger than W_p of PUN transistors.

NOR



To improve the charge speed, W_p must be larger than W_n of PDN transistors.

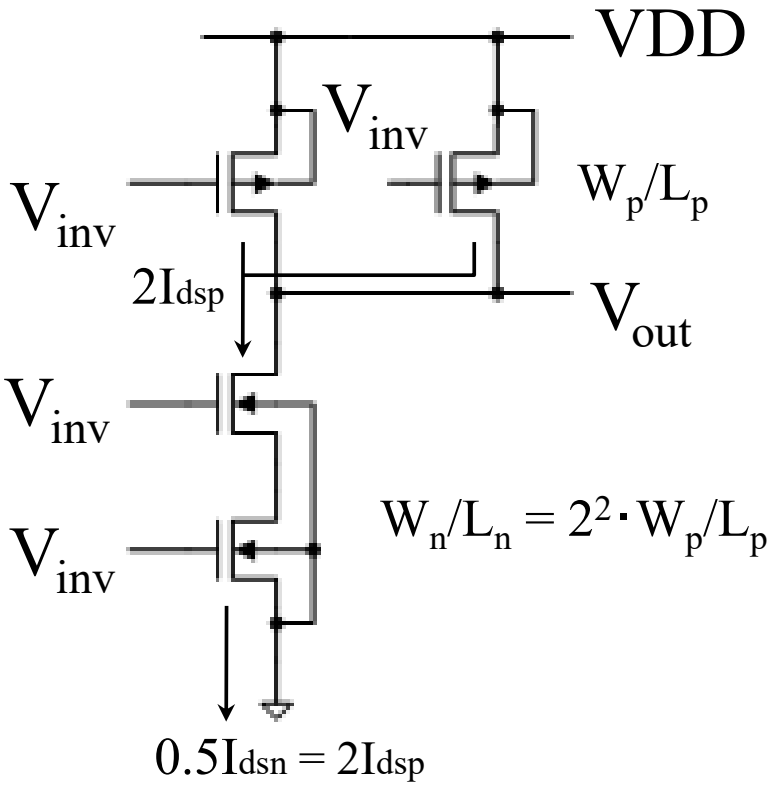
Gate width of MOSFET



When $\beta_n = \beta_p$,

$V_{inv} = VDD/2.$

$$\frac{W_n}{L_n}\mu_n = \frac{W_p}{L_p}\mu_p$$



When $0.5\beta_n = 2\beta_p$,

$V_{inv} = VDD/2.$

$$\frac{W_n}{L_n}\mu_n = 2^2\frac{W_p}{L_p}\mu_p$$

Optimization of L_n, L_p, W_n, W_p of multi-input gates

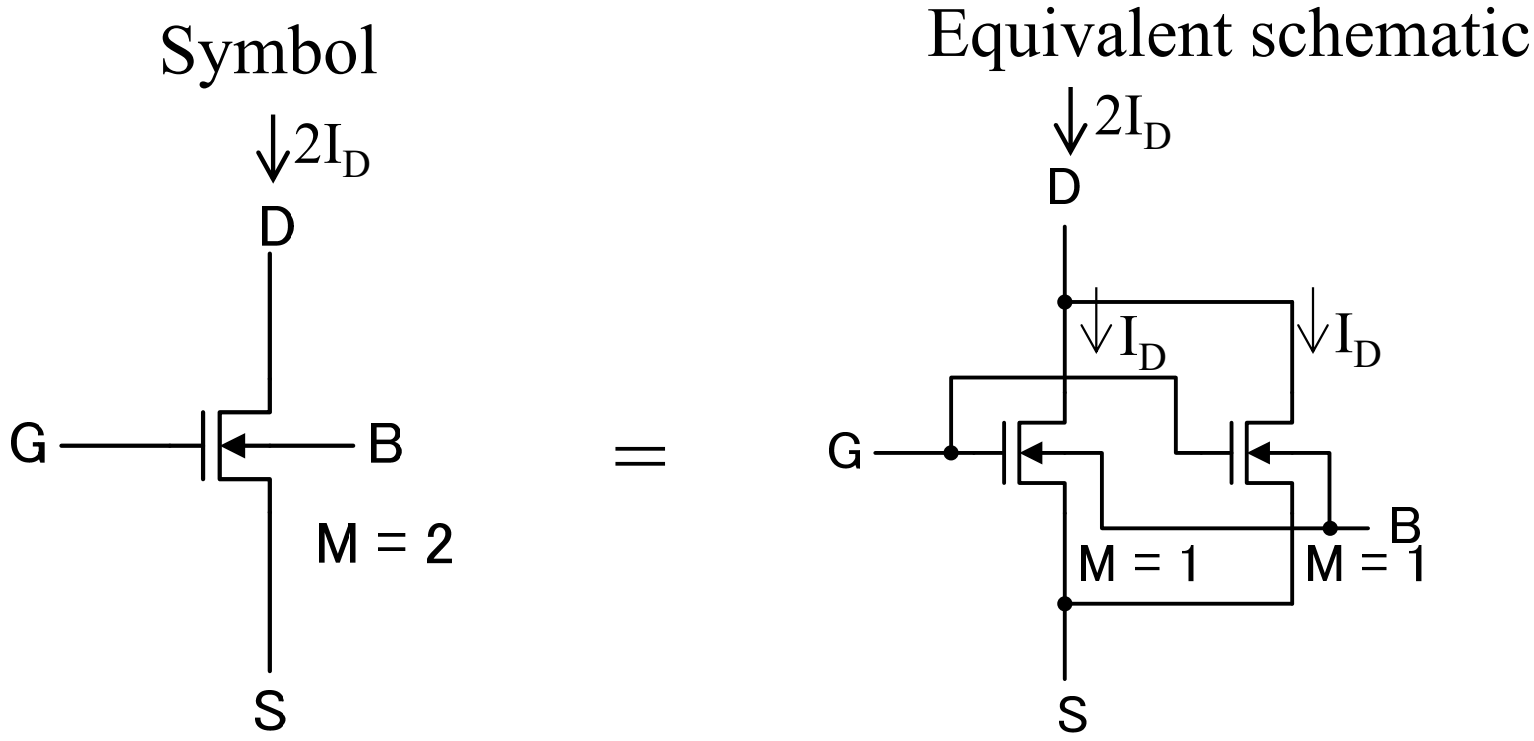
When $L_n = L_p$, $\dfrac{W_p}{W_n} = \dfrac{\mu_n}{\mu_p} = 1.5 \sim 3$ (for inverter)

Optimum value of Wp/Wn

Number of inputs	1	2	N
Inverter	μ_n/μ_p		
NAND		$(\mu_n/\mu_p)/2^2$	$(\mu_n/\mu_p)/N^2$
NOR		$(\mu_n/\mu_p)2^2$	$(\mu_n/\mu_p)N^2$

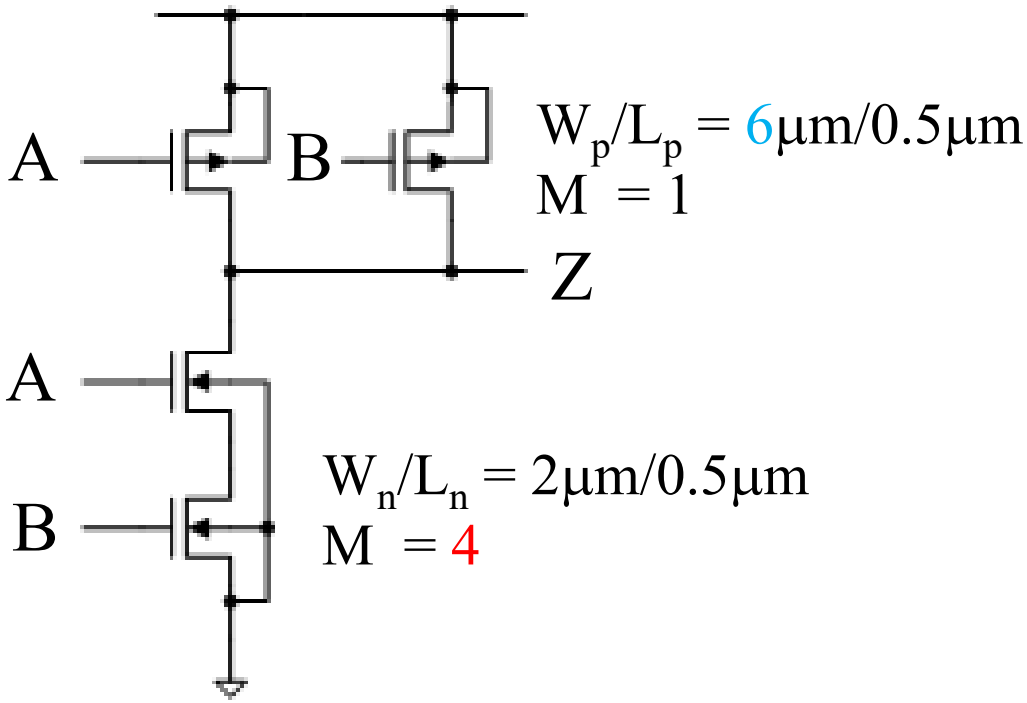
Number of parallel connections

The parameter M is defined as number of parallel connections.
M is called a multiplier of MOSFET.
When N is an input number of NAND, you may set a value of N^2 as M of n-ch MOSFET.



Example of NAND design

$L_n = L_p = 0.5\mu m,\ \mu_n/\mu_p = 3.0$



$$0.5\beta_n = 2\beta_p$$

$$\beta_n = 2^2\beta_p$$

$$\mu_n C_o \frac{W_n}{L_n} = 2^2 \mu_p C_o \frac{W_p}{L_p}$$

$$\frac{\mu_n}{\mu_p}\frac{W_n}{L_n} = 2^2 \frac{W_p}{L_p} = M\frac{W_p}{L_p}$$