

Integrated circuit A and B

Microelectronics Research Lab. (MeRL)

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0.1 Course information

LSIs designed in MeRL

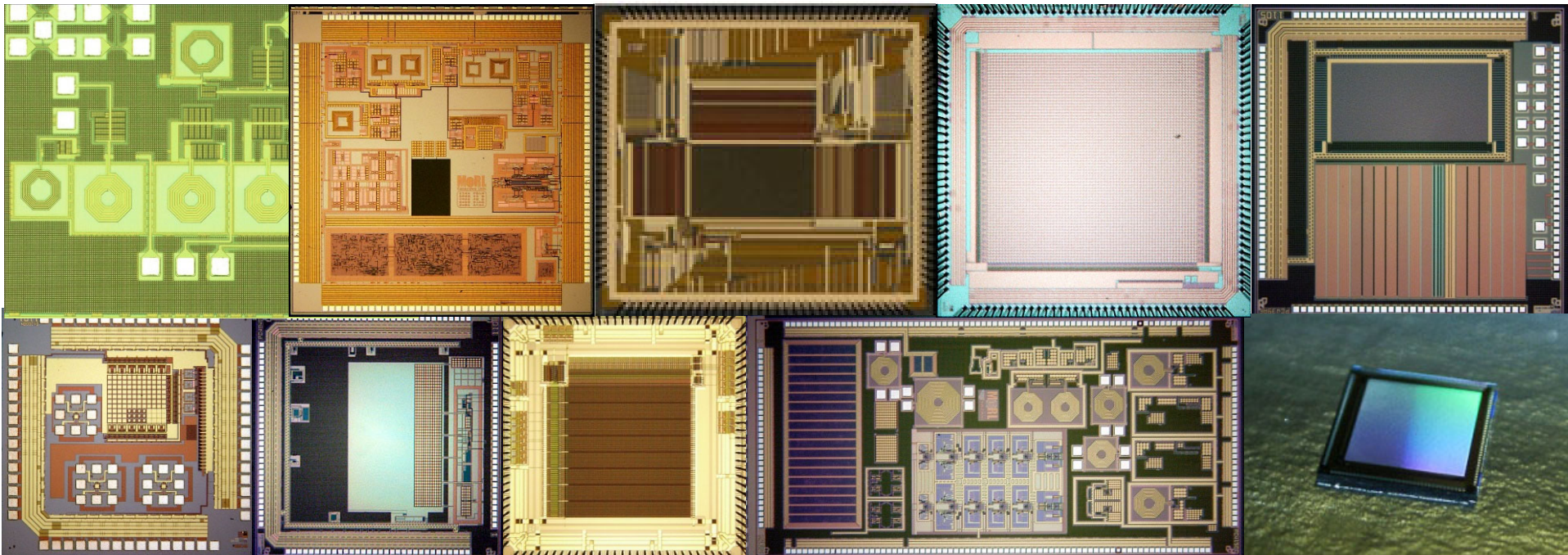
Low noise amp.

Resistive memory

Color sensor

UHF transceiver

Particle sensor



Tactile sensor

Phase change memory

Micro-display

Sensor RF-ID

Dual band transceiver

LSI (Large Scale Integration): The terms of LSI and VLSI are synonyms terms of IC. 3

Integration of functions

General-purpose IC

Microprocessor

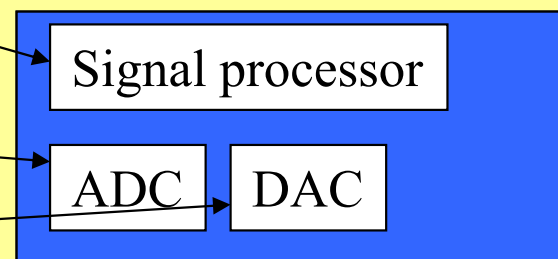
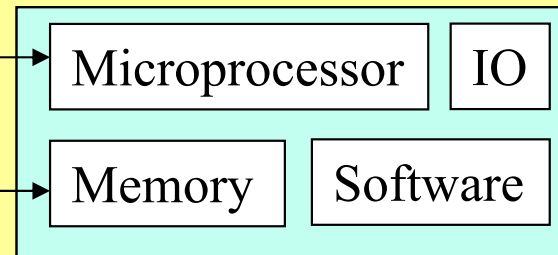
Memory

Signal processor

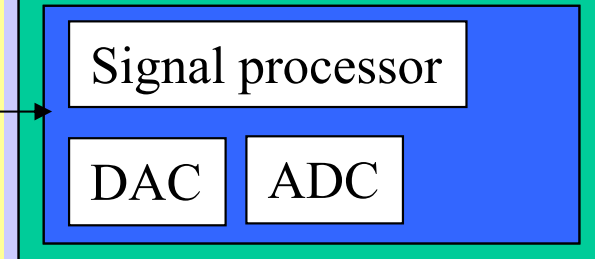
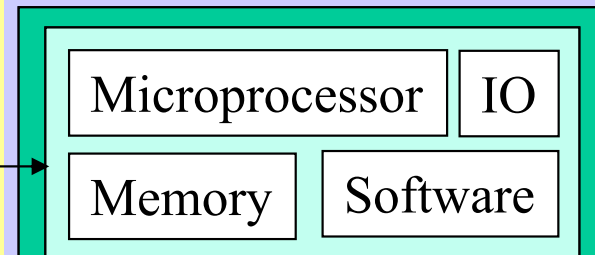
ADC

DAC

Application specific standard product



SoC (System on a Chip) or Custom LSI



DAC: Digital-to-Analog Converter
ADC: Analog-to-Digital Converter
IO: Input/output system

Microcontroller, Digital audio, Image processor...

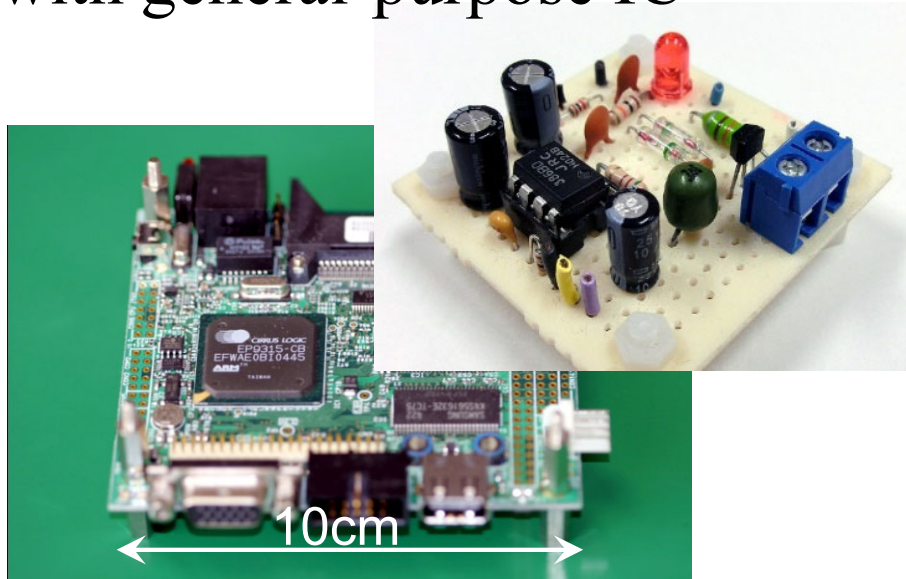
Smartphone, DTV, Electronic money...

Designed in semiconductor companies

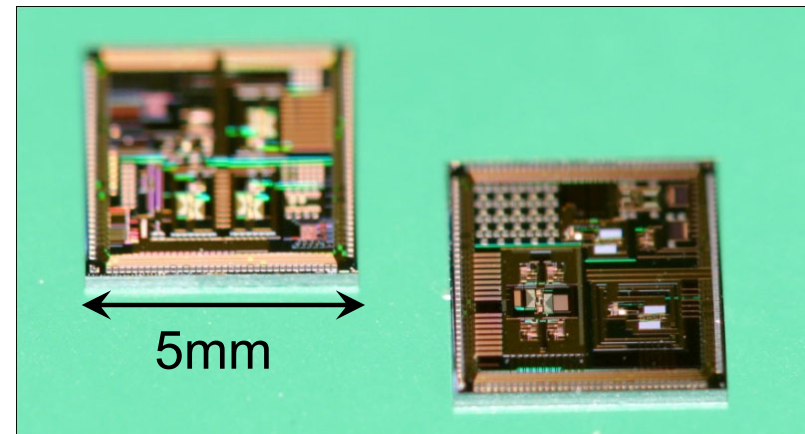
Designed by users

Advantages of custom LSI

PCB (Printed Circuit Board)
with general-purpose IC



Custom LSI

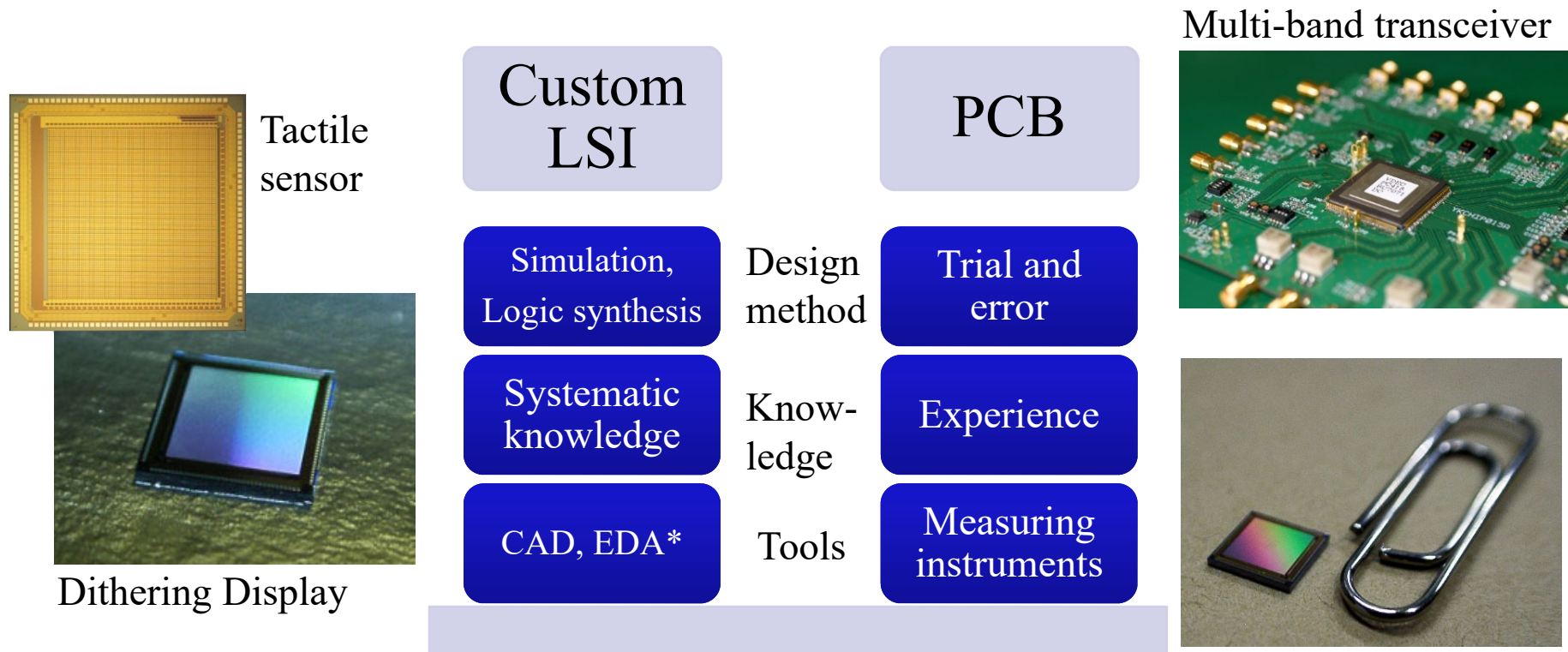


Speed < 50MHz
Number of wires < 1000
Low flexibility of design
Short TAT*

Speed > 100GHz
Number of wires ~ Unlimited
High flexibility of design
Long TAT*

* TAT (Turn around Time) = Work period 5

Comparison of design process

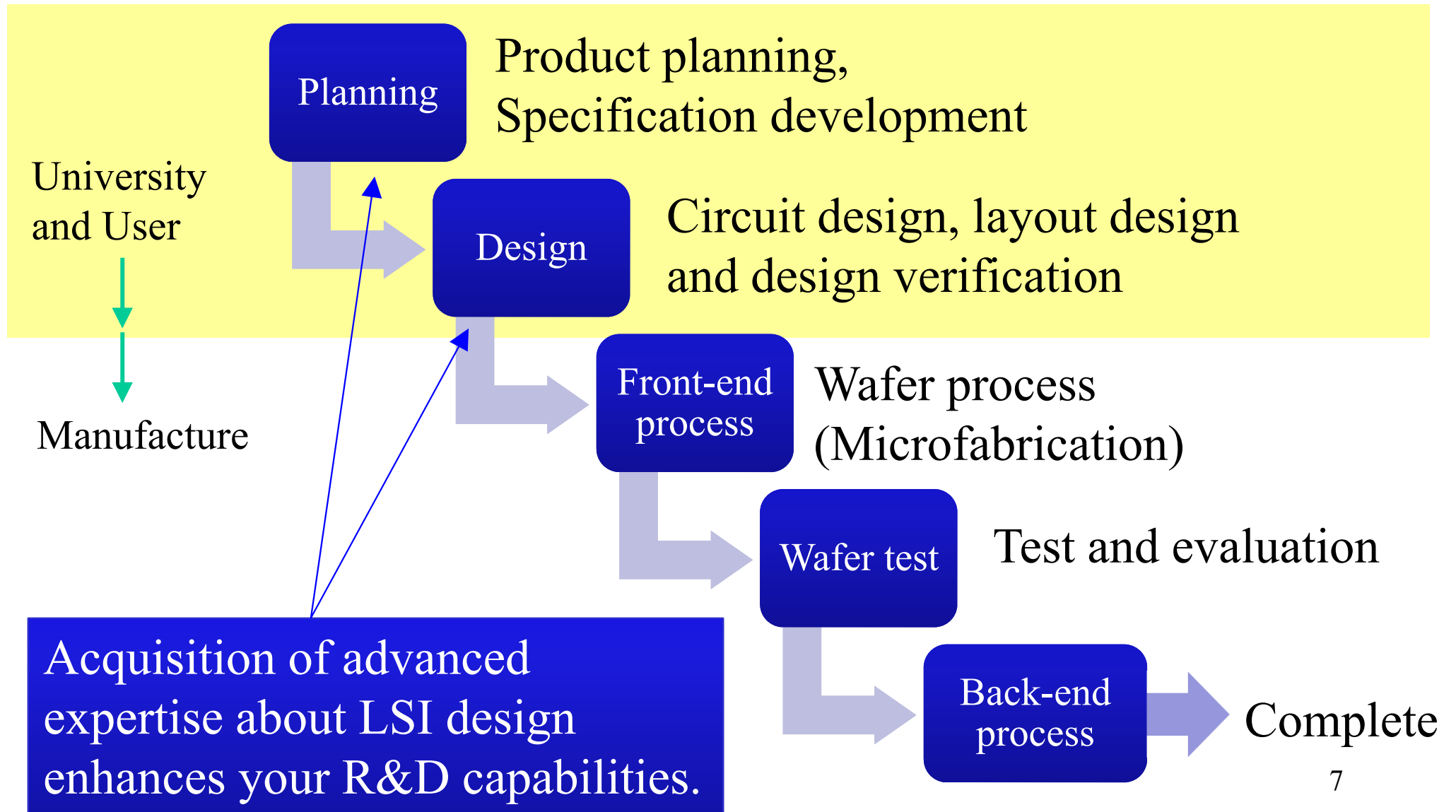


You can use the knowledge that you learn in college.

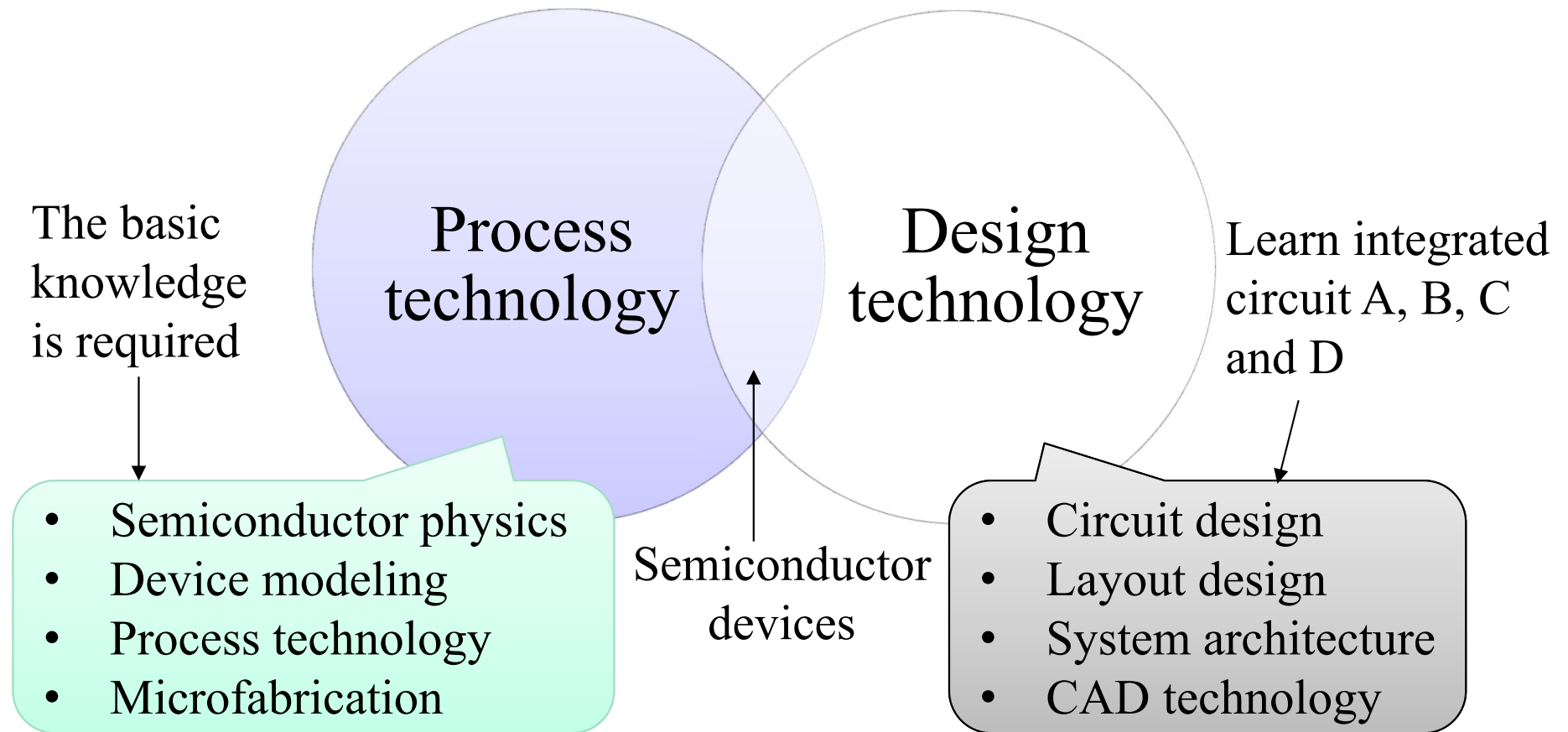
Accumulated know-how is required.

* CAD: Computer Aided Design, EDA: Electronic Design Automation

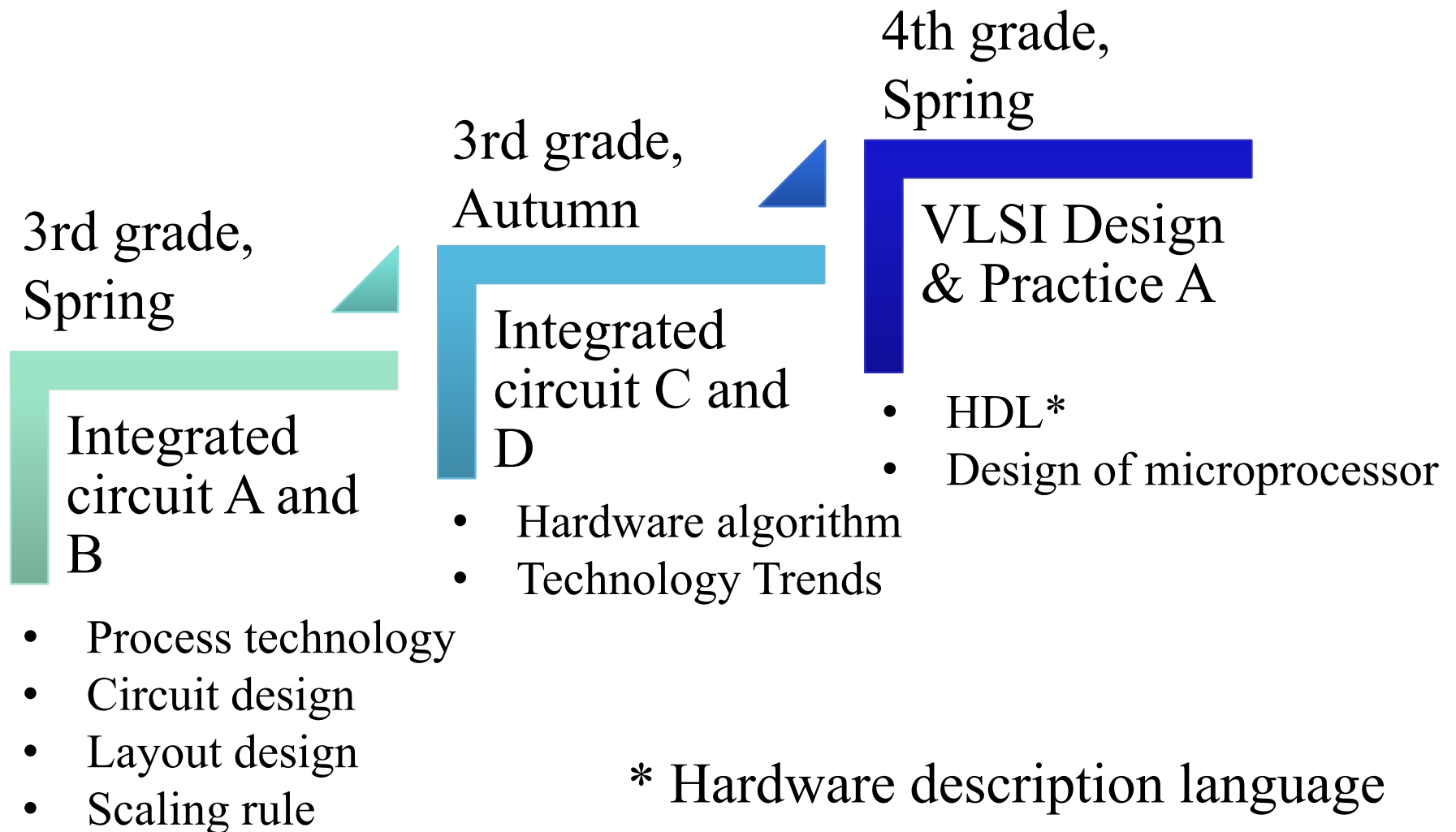
Modern LSI development process



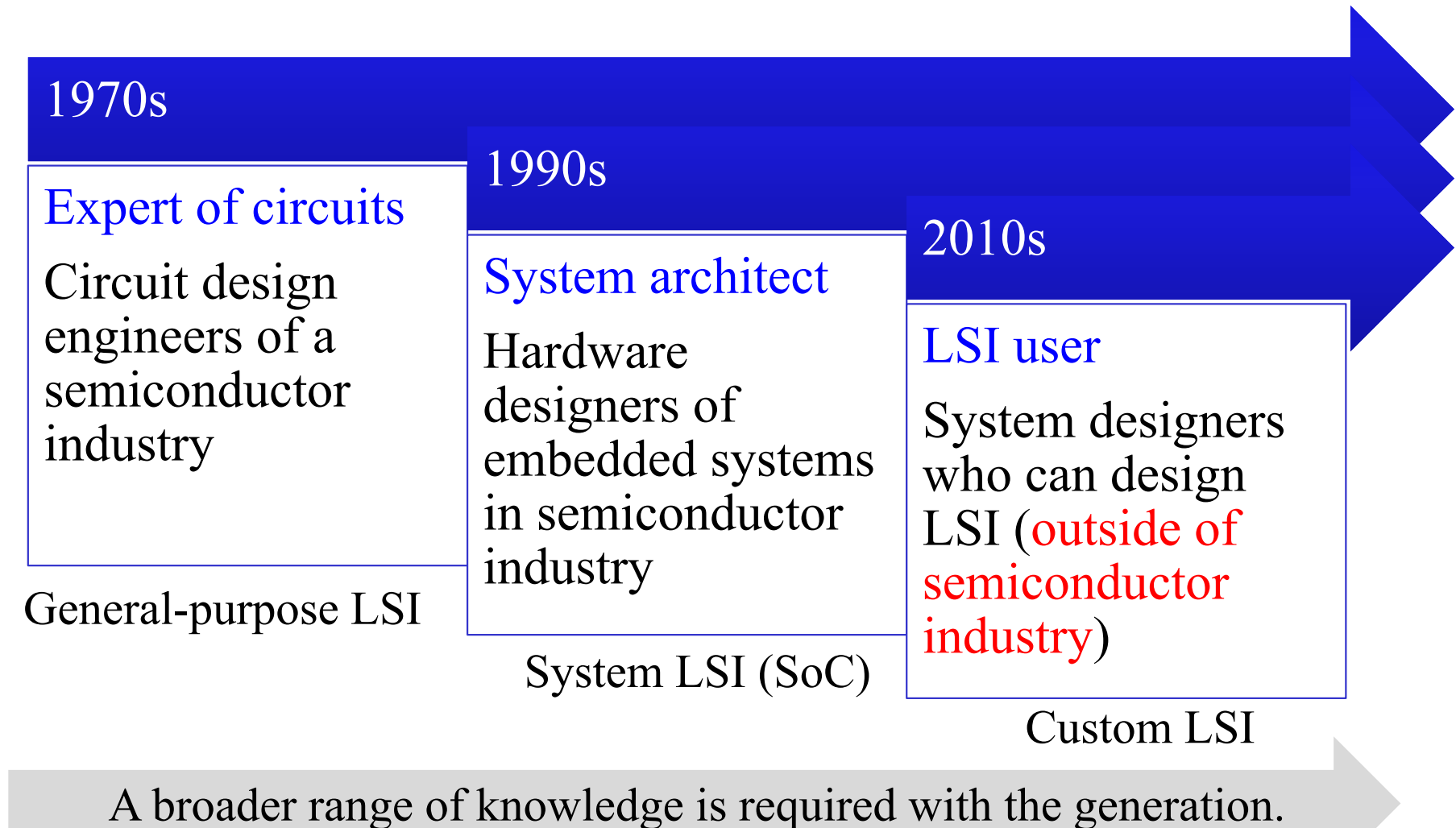
Academic framework of Microelectronics



Curriculum of LSI design course



Vicissitude of LSI designers



Hierarchical design of LSI

Abstraction level	Design target	Description method
System level (H/W and S/W)	System architecture Software/Hardware partitioning Communication protocol Embedded software	High-level programming language SystemC SystemVerilog
Sub-system level (CPU, Memory, Arithmetic unit , and so on)	Hardware algorithm Software interface Communication interface	Flowchart State Transition Diagram Behavior level HDL Logic circuit, Schematic circuit
Gate level	Logic function	Logic circuit, Truth table State Transition Diagram Structure level HDL
Transistor level	Logic gate, RF circuit, Clock circuit	Schematic circuit SPICE netlist
Physical level (Layout)	Cell library, Circuit block	Layout diagram (GDS-II)

Course objectives

- Contents
 - Design of **CMOS (*) logic** and transistor circuit
 - You do not need to learn the design of the transistor circuits, if you can use the logic synthesis to design the logic circuits. However, you must learn the principle of the transistor circuits to understand how to use the electronic design automation tools.
 - * **CMOS: Complementary Metal-Oxide-Semiconductor**
 - Estimation of the performance of CMOS logic, such as an operating speed, a power consumption.
- Students will be able to
 - design **the CMOS combinational logic and the CMOS sequential logic**
 - understand **the design flow** and required CAD software
 - understand **the method of the layout design**
 - estimate **the performance of the CMOS logic**
 - understand **the scaling rule and the scaling effect**

References

- Book
 - ウエスト&ハリス著「CMOS VLSI回路設計(基礎編)」(丸善出版) ISBN978-4-621-08721-3
- Course materials
 - Download from
<http://jaco.ec.t.kanazawa-u.ac.jp/kitagawa/edu/>
- Recommended reading
 - よくわかる!半導体 2012年版 (ICガイドブック) 社団法人電子情報技術産業協会編(古本を探す必要あり)
 - 西久保靖彦著, 図解入門よくわかる最新半導体の基本と仕組み[第2版](秀和システム)

Course policy

1. Download the lecture slide of the on the web site shown in the previous page.
2. The course is provided by face-to-face classes and online classes simultaneously.
3. If you have a question, post the question on the BBS or the timeline of WebClass (Click the icon of a pen.)
4. Submit the assignment by the deadline.
 - Academic misconduct and scholastic dishonesty such as a plagiarizing or cheating on examinations can be assigned a penalty based on the university regulations.

Grading

- Grading policies

- ~~— Regular assignments (20%), Design practice (20%), Final exam (60%) Assignments (100%)~~

- ~~— In the final exam, you may refer to any book, notebook, and handouts.~~

- ~~— The scores of your report taken will become invalidated, if you are late to submit the report.~~

- However, even if the submission is delayed, it will be treated as a legitimate submission, when you can prove that you are not responsible. For example, an illness, an official event.

- ~~• Make-up exam~~

- ~~— The make-up exam will be carried out, if you cannot take the final exam due to unavoidable circumstances.~~

- ~~• Study for an examination~~

- ~~— Your note and annotation in every class will be helpful in your review and studying for the exam. The course materials is incomplete for the self-learning.~~

Q & A

- During class
 - Feel free anytime in the class.
 - The remote students may use the comment section in the online meeting tool.
- Office hours
 - 5th period on Wednesday
 - Request for an appointment.
- Timeline on WebClass
 - For questions about the lecture.
- Email
 - For questions about your grading, attendance.
 - kitagawa@merl.jp