

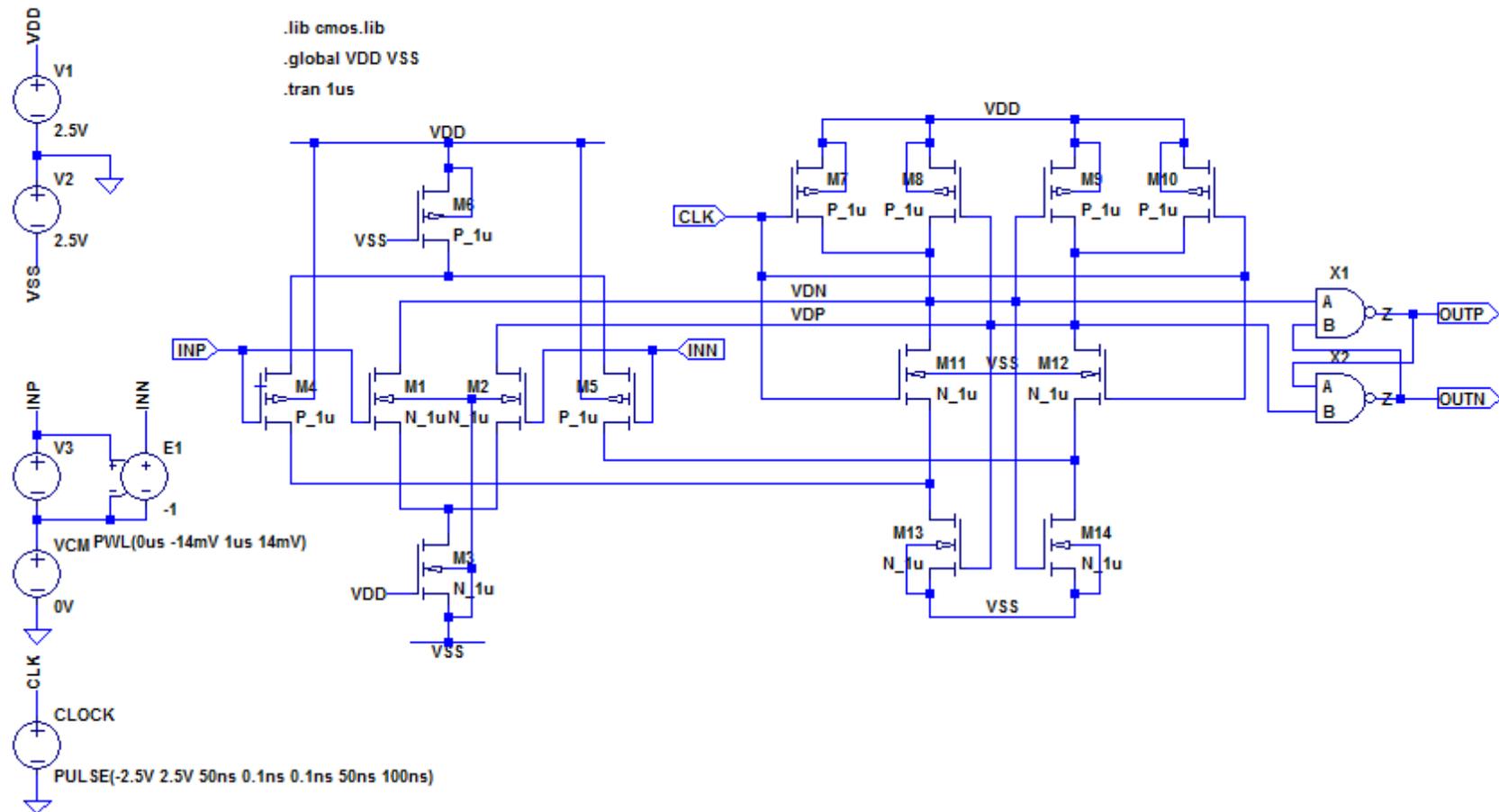
Lab. 15

CHARACTERIZATION OF CLOCKED COMPARATOR

1. Characterization

- Carry out the TRAN analysis of the clocked comparator and attach the simulation results to your report.
 - $V(\text{inp})$, $V(\text{inn})$, $V(\text{outp})$, $V(\text{vdn})$, $V(\text{vdp})$, and $V(\text{clk})$
- Evaluate the comparison accuracy by simulation.
 - The accuracy depends on the clock frequency. Try to operate at $f_{\text{clk}} = 10\text{MHz}$ ($T_{\text{period}} = 100\text{ns}$).
 - The accuracy depends on the common mode voltage too. Evaluate the comparison accuracy for $V_{\text{CM}} = -1.0\text{V}$, 0.0V , and 1.0V .

Schematic



Clock pulse and input voltage

Independent Voltage Source - CLOCK

Functions

- (none)
- PULSE(V1 V2 Tdelay Trise Tfall Ton Period Ncycles)
- SINE(Voffset Vamp Freq Td Theta Phi Ncycles)
- EXP(V1 V2 Td1 Tau1 Td2 Tau2)
- SFFM(Voff Vamp Fcar MDI Fsig)
- PWL(t1 v1 t2 v2...)
- PWL FILE:

Vinitial[V]:

Von[V]:

Tdelay[s]:

Trise[s]:

Tfall[s]:

Ton[s]:

Tperiod[s]:

Ncycles:

Make this information visible on schematic

Independent Voltage Source - V3

Functions

- (none)
- PULSE(V1 V2 Tdelay Trise Tfall Ton Period Ncycles)
- SINE(Voffset Vamp Freq Td Theta Phi Ncycles)
- EXP(V1 V2 Td1 Tau1 Td2 Tau2)
- SFFM(Voff Vamp Fcar MDI Fsig)
- PWL(t1 v1 t2 v2...)
- PWL FILE:

time1[s]:

value1[V]:

time2[s]:

value2[V]:

time3[s]:

value3[V]:

time4[s]:

value4[V]:

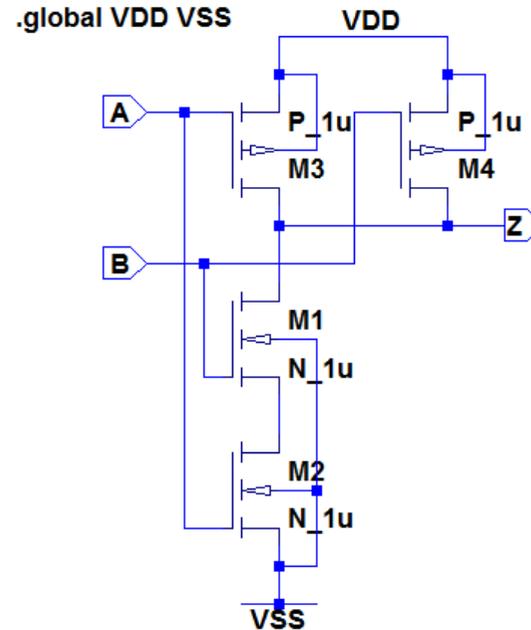
Make this information visible on schematic

Change the Value1 and Value2 to evaluate the comparison accuracy.

MOSFET parameters

MOSFET	L(m)	W(m)	M	AD, AS(m ²)	PD, PS(m)	W/L
M1, M2	2u	10u	2	30p	16u	10
M3	4u	20u	2	60p	26u	10
M4, M5	2u	10u	6	30p	16u	30
M6	4u	20u	6	60p	26u	30
M7-M10	2u	10u	3	30p	16u	15
M11-M14	2u	10u	1	30p	16u	5

NAND2 schematic



MOSFET	L(m)	W(m)	M	AD, AS(m ²)	PD, PS(m)	W/L
M1, M2	1u	5u	4	15p	11u	5
M3, M4	1u	15u	1	45p	21u	15