

Lab. 13 Example solution

DESIGN AND CHARACTERIZATION OF FULL-DIFFERENTIAL OPA

1. Design of full-differential OPA

Folded-cascode differential amplifier

$$GBP = 40\text{MHz} \quad CL = 1.0\text{pF}$$

$$gm1 = \sqrt{2\beta_1 I_{DS1}} = GBP \cdot CL = 2\pi \cdot 40\text{MHz} \cdot 1.0\text{pF} = 251\mu\text{S}$$

$$\beta_1 = \frac{gm1^2}{2I_{DS1}}$$

$$\left(\frac{W}{L}\right)_1 = \frac{1}{\mu_n C_{OX}} \frac{gm1^2}{2I_{DS1}} = \frac{1}{98\mu\text{A}/\text{V}^2} \frac{(251\mu\text{S})^2}{2 \cdot 10\mu\text{A}} = 32.1 \approx 32 = \frac{64}{2} = \left(\frac{16}{2}\right) \cdot 4$$

CMFB

When the input voltages V_{in}^+ and V_{in}^- are equal to the common mode voltage, the output voltage of CMFB must be close to the gate voltage of M9 and M10 of the full-differential amplifier. Therefore, when the bias current of M5-M12 is the same as M9 and M10, the size of M5-M12 of the CMFB can be set at the same size as M9 and M10 of the full-differential amplifier.

1. Design of full-differential OPA

Folded-cascode differential amplifier

| MOSFET | L(m) | W(m) | M | AD, AS(m ²) | PD, PS(m) | W/L |
|-----------------|------|------|---|-------------------------|-----------|-----|
| M1, M2 | 2u | 16u | 4 | 48p | 22u | 32 |
| M3, M4, M7-M10 | 2u | 10u | 3 | 30p | 16u | 15 |
| M5, M6, M11-M13 | 2u | 10u | 1 | 30p | 16u | 5 |

CMFB

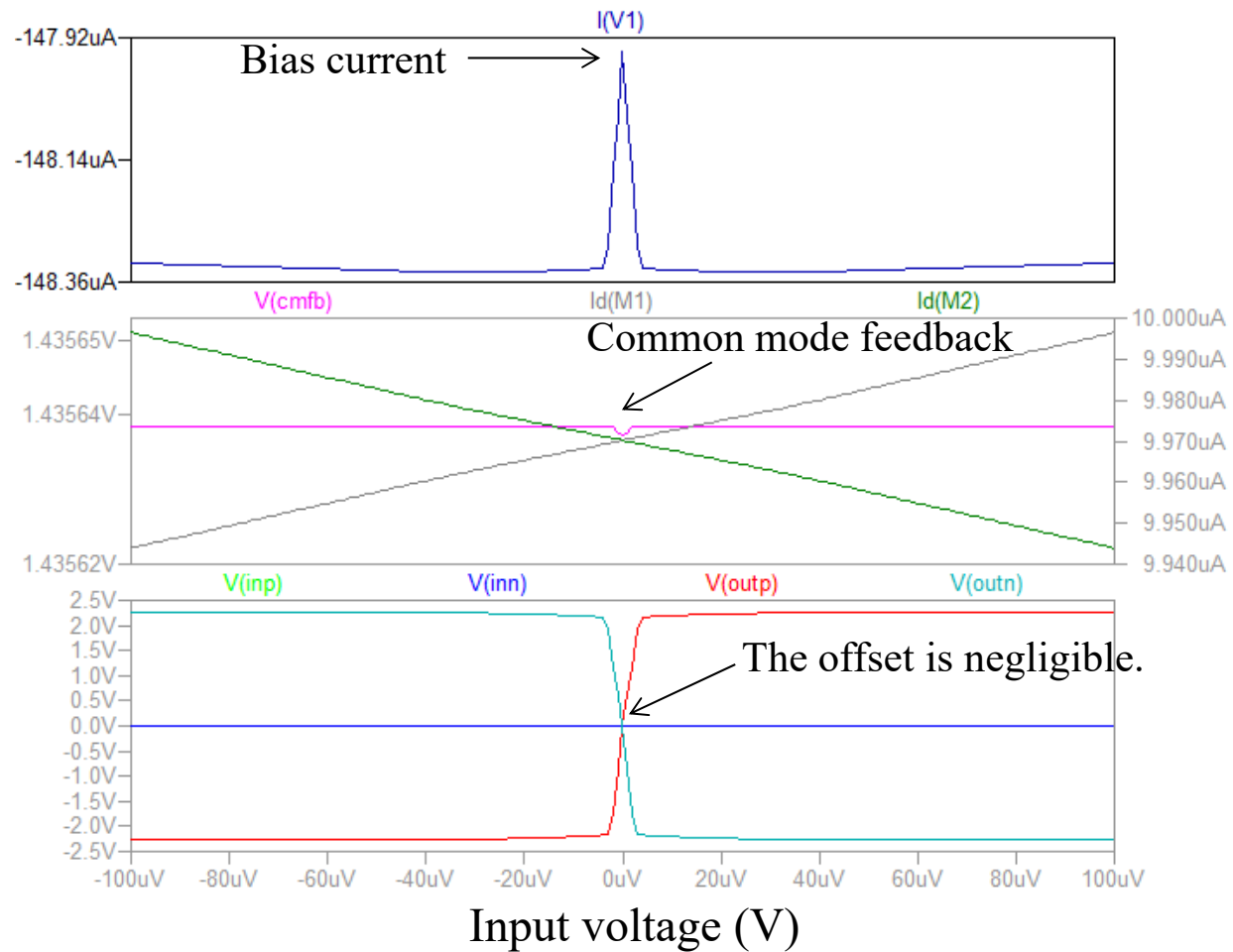
| MOSFET | L(m) | W(m) | M | AD, AS(m ²) | PD, PS(m) | W/L |
|---------|------|------|---|-------------------------|-----------|-----|
| M1-M4 | 2u | 16u | 8 | 48p | 22u | 64 |
| M5-M12 | 2u | 10u | 3 | 30p | 16u | 15 |
| M13-M16 | 2u | 10u | 1 | 30p | 16u | 5 |

Table III

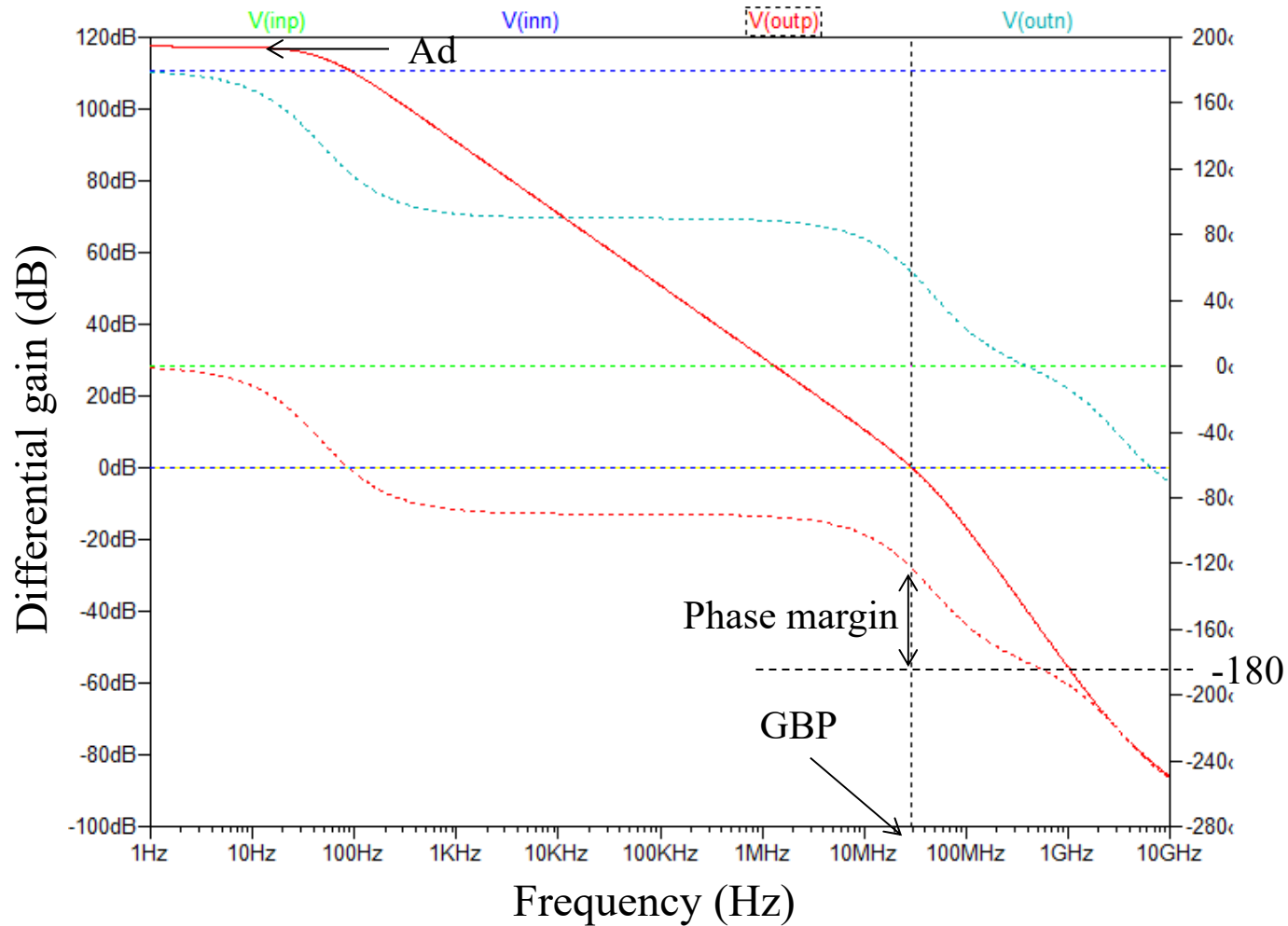
- The specification estimated by the simulation.

| Parameter | Unit | Value | Remarks |
|--------------------|--------|---------|------------|
| GBP | Hz | 29.5MEG | CL = 1.0pF |
| A_d | dB | 117 | @ 10Hz |
| Phase Margin | degree | 56.9 | |
| Slew Rate | V/us | 11.1 | CL = 1.0pF |
| Total Bias Current | A | 148.0u | |
| Reference Current | A | 9.97u | $I_{SS}/2$ |

DC characteristic



AC characteristic



Input pulse

Independent Voltage Source - V4

Functions

- (none)
- PULSE(V1 V2 Tdelay Trise Tfall Ton Period Ncycles)
- SINE(Voffset Vamp Freq Td Theta Phi Ncycles)
- EXP(V1 V2 Td1 Tau1 Td2 Tau2)
- SFFM(Voff Vamp Fcar MDI Fsig)
- PWL(t1 v1 t2 v2...)
- PWL FILE:

Vinitial[V]:
Von[V]:
Tdelay[s]:
Trise[s]:
Tfall[s]:
Ton[s]:
Tperiod[s]:
Ncycles:

Make this information visible on schematic:

DC Value

DC value:

Make this information visible on schematic:

Small signal AC analysis(.AC)

AC Amplitude:
AC Phase:

Make this information visible on schematic:

Parasitic Properties

Series Resistance[Ω]:
Parallel Capacitance[F]:

Make this information visible on schematic:

Note: Select none as a function and set the DC value at zero before the AC analysis.

TRAN response

