

# 9. Voltage references

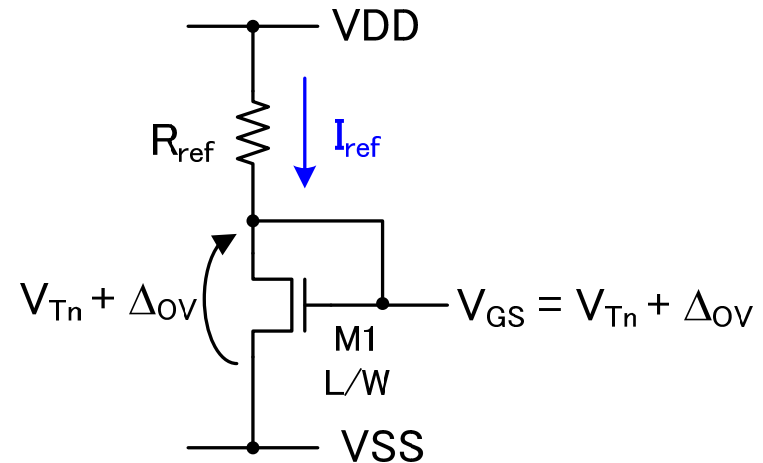
A voltage and current reference are used for the reference of bias circuit, DAC and ADC.

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# 9.1 Simple reference circuits

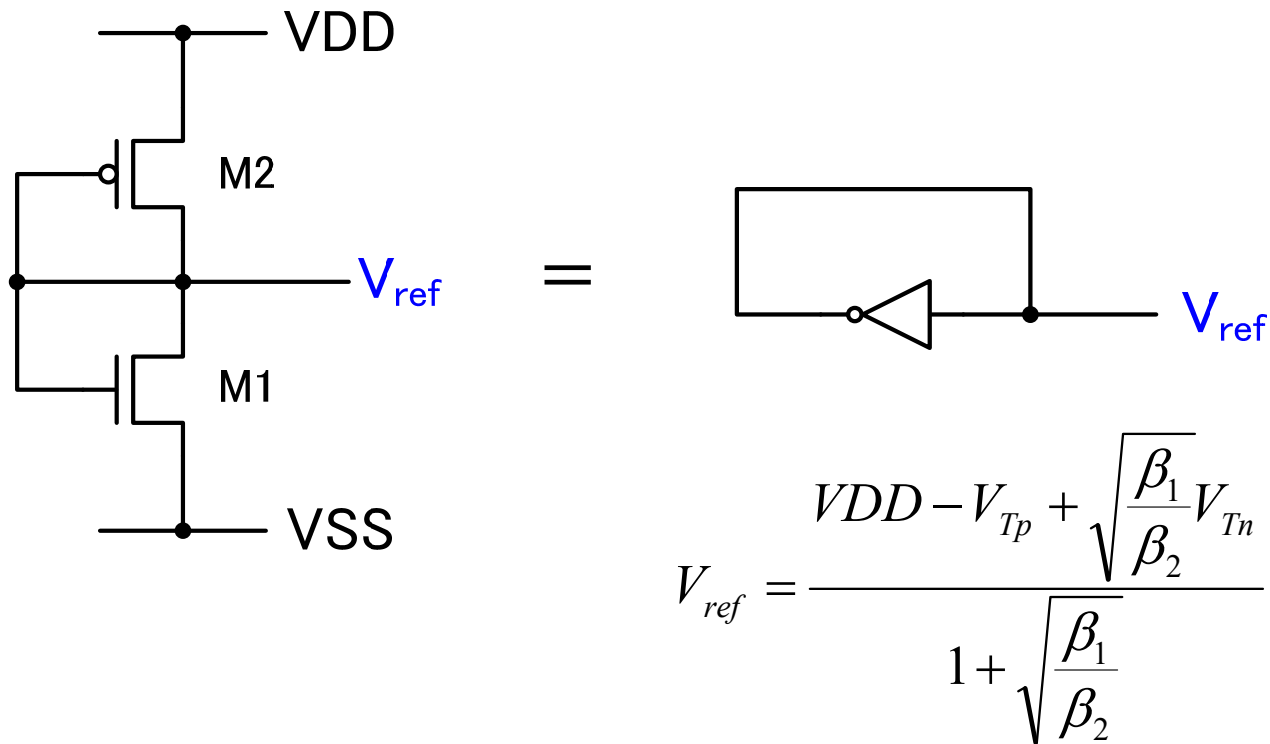
# R-MOSFET voltage reference

$$\begin{aligned} I_{ref} &= \frac{1}{R_{ref}} (VDD - V_{Tn} - \Delta_{OV}) \\ &= \frac{1}{R_{ref}} (VDD - V_{Tn} - \sqrt{\frac{2I_{ref}}{\beta_n}}) \\ &\approx \frac{1}{R_{ref}} (VDD - V_{Tn}) \quad \text{if } I_{ref} \text{ is small enough.} \end{aligned}$$



- Bad stability against the temperature variation, because the temperature coefficient of  $I_{ref}$  depends on the temperature coefficient of  $R_{ref}$  and  $V_{Tn} + \Delta_{OV}$ .
- No stability against  $VDD$ , because  $I_{ref}$  and  $V_{GS}$  depend on  $VDD$ .

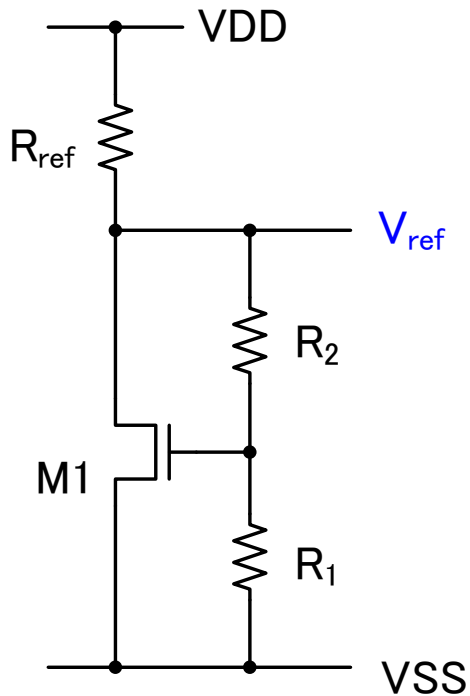
# MOSFET Driver



- No stability against VDD, because  $V_{ref}$  depends on VDD.
- The temperature coefficient of  $V_{Tn}$ ,  $V_{Tp}$  can be canceled by a temperature coefficient of  $\beta_1/\beta_2$ .

# Threshold-Voltage Multiplier

This circuit has a NFB loop in which the decrease of  $I_{ref}$  causes the increase of  $V_{GS}$ .



$$V_{GS1} = \frac{R_1}{R_1 + R_2} V_{ref}$$

$$V_{ref} = V_{GS1} \cdot \left( \frac{R_2}{R_1} + 1 \right)$$

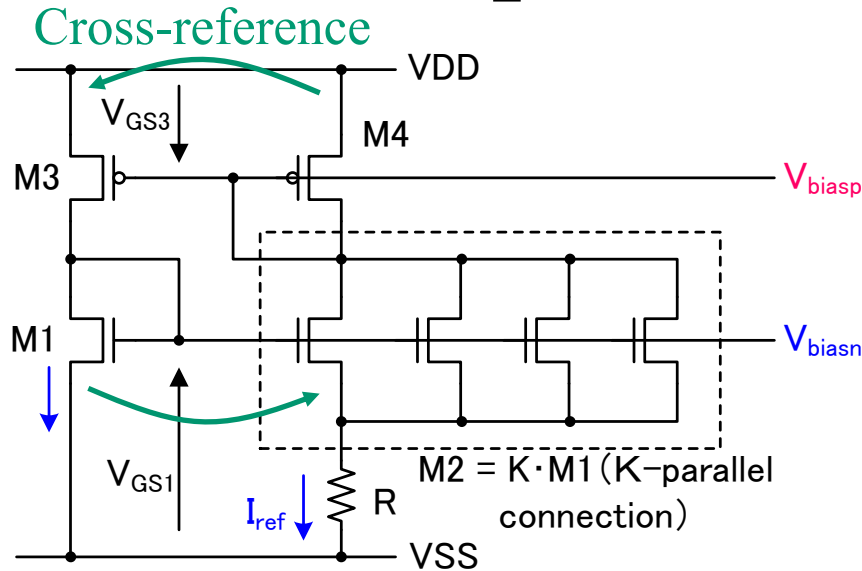
If  $I_{ref}$  is small enough,

$$V_{ref} \cong V_{Tn} \cdot \left( \frac{R_2}{R_1} + 1 \right)$$

$V_{ref}$  does not depend on VDD.

## 9.2 Beta-Multiplier Reference (BMR)

# Principle of BMR circuit



$$\begin{cases} I_{DS4} = I_{DS3} \\ I_{DS1} = I_{DS2} \equiv I_{ref} \\ V_{GS1} = V_{GS2} + I_{ref}R \end{cases}$$

i.e.

$$\beta_2 = \beta_1 \rightarrow I_{ref}R = 0 (V_{GS1} = V_{GS2})$$

$$\beta_2 = K\beta_1 \rightarrow I_{ref}R \neq 0 (V_{GS1} = V_{GS2} + I_{ref}R)$$

(BMR: Beta-Multiplier Reference)

$$I_{DS1} = \frac{\beta_1}{2} (V_{GS1} - V_{Tn})^2$$

$$I_{DS2} = \frac{\beta_2}{2} (V_{GS2} - V_{Tn})^2 = K \frac{\beta_1}{2} (V_{GS2} - V_{Tn})^2$$

$$I_{DS1} = I_{DS2} = I_{ref}$$

$$I_{ref} = \frac{1}{R} (V_{GS1} - V_{GS2}) = \frac{1}{R^2} \frac{2}{\beta_1} \left(1 - \frac{1}{\sqrt{K}}\right)^2$$

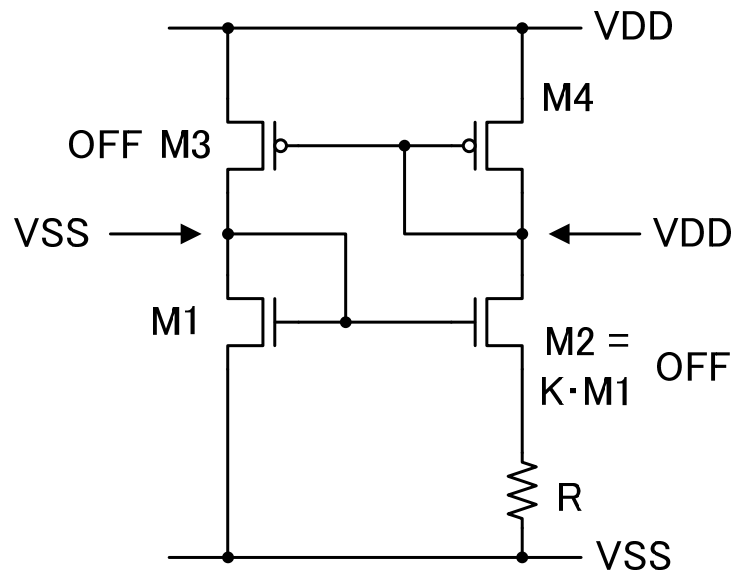
I<sub>ref</sub> is independent on VDD.

The temperature coefficient of I<sub>ref</sub> depends on the temperature coefficients of R and β<sub>1</sub>.

# Start-up circuit (1)

BMR has two operating state because of a positive feedback.

⇒ The initial state should be determined by the start-up circuit.

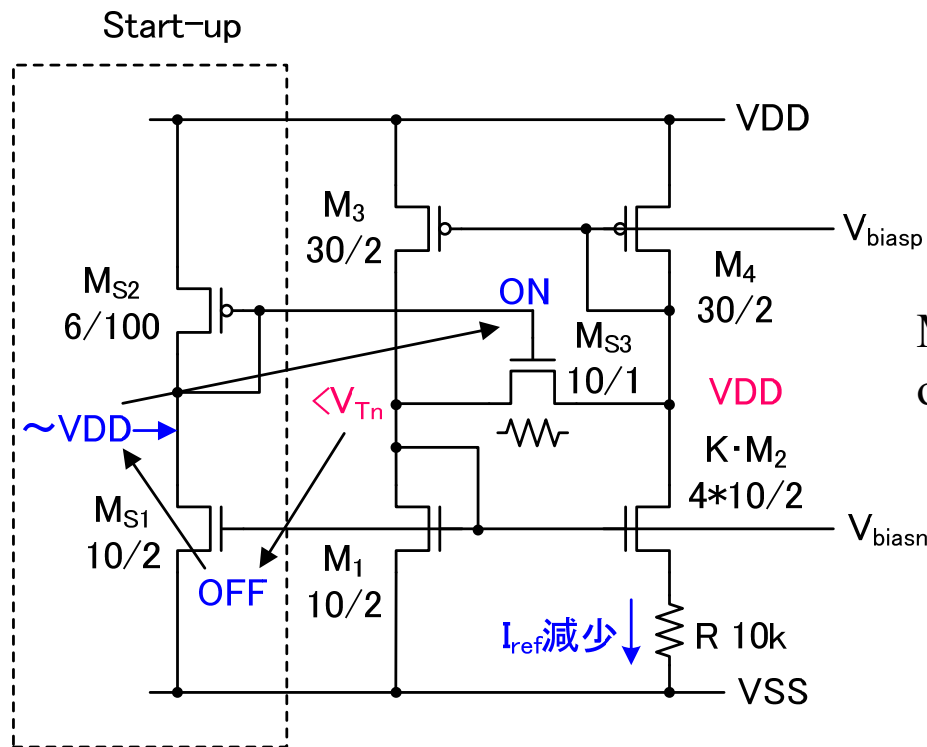


" $I_{\text{ref}} = 0$ " is a solution of the circuit equation too.



# Start-up circuit (2)

The drain potential of M1-M4 is equalized by MS3.



$$I_{DS\_MS1} = I_{DS\_MS2} = I_{ref} \text{ (Normal operation)}$$

$$V_{GS\_MS2} = \sqrt{\frac{2I_{ref}}{\beta_{MS2}}} + V_{Tp}$$

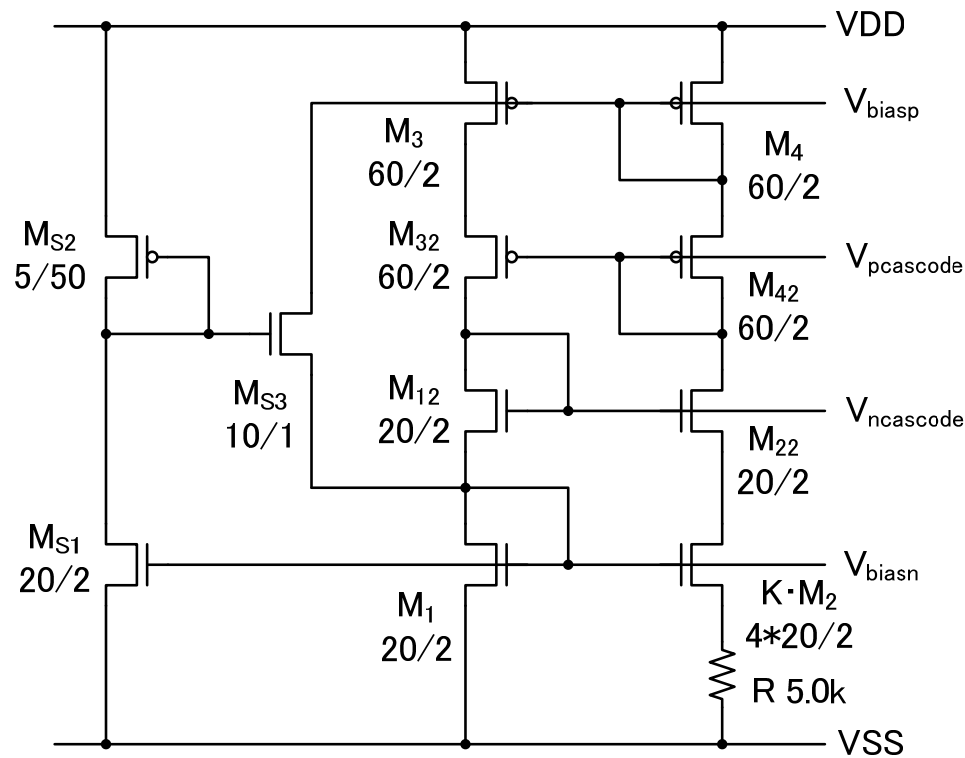
MS3 should be turned off in the normal operation.

$$V_{GB\_MS3} = VDD - V_{GS\_MS2} - VSS$$

$$= (VDD - VSS) - |V_{Tp}| - \sqrt{\frac{2I_{ref}}{\beta_{MS2}}} < V_{Tn}$$

NOTE: The gate length L of MS2 is often very long, if  $I_{ref}$  is small value. 9

# Design example of cascode BMR



For  $I_{ref} = 20\mu A$ ,

$$\Delta_{OV} = \sqrt{\frac{2I_{ref}}{\beta_1}} = \sqrt{\frac{2 \cdot 20\mu}{98\mu \cdot 10}} = 0.20V$$

$$R = \sqrt{\frac{2}{I_{ref}\beta_1} \left(1 - \frac{1}{\sqrt{K}}\right)}$$

$$= \sqrt{\frac{2}{20\mu \cdot 98\mu \cdot 10} \left(1 - \frac{1}{2}\right)} = 5.0k\Omega$$

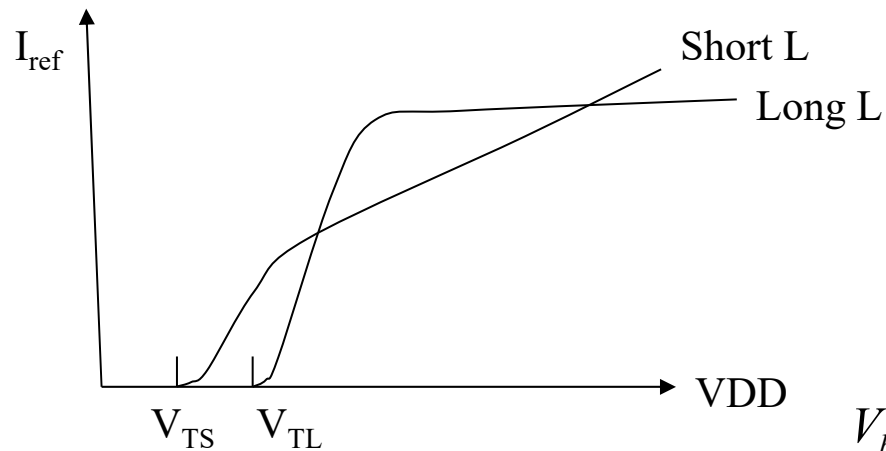
$$\beta_{MS2} < \frac{2I_{ref}}{(VDD - VSS - |V_{Tp}| - V_{Tn})^2}$$

$$= \frac{2 \cdot 20\mu}{(5.0 - 1.6)^2} = 3.46\mu$$

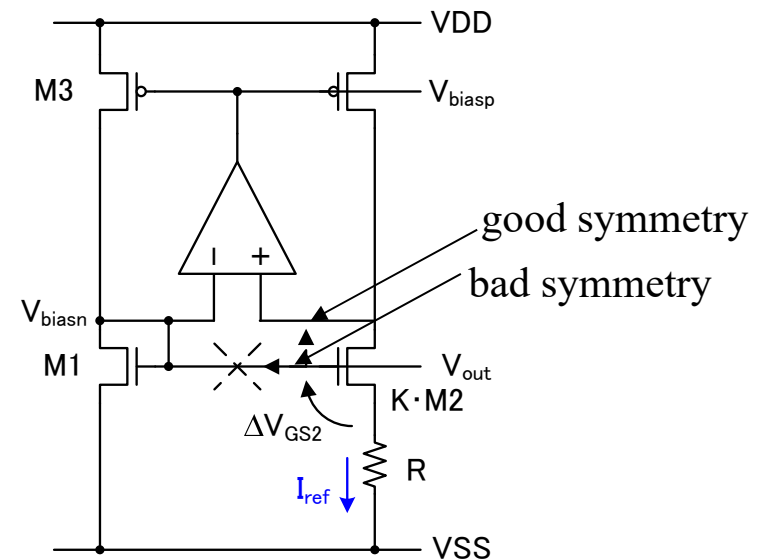
$$\frac{W_{MS2}}{L_{MS2}} < \frac{3.46\mu}{33\mu} = 0.105$$

# Voltage regulation

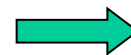
Short channel MOSFET vs.  
Long channel MOSFET



$I_{ref}$  depends on the drain voltage, because the saturation of  $I_{DS}-V_{DS}$  characteristics of the short channel MOSFET is not distinguished clearly.



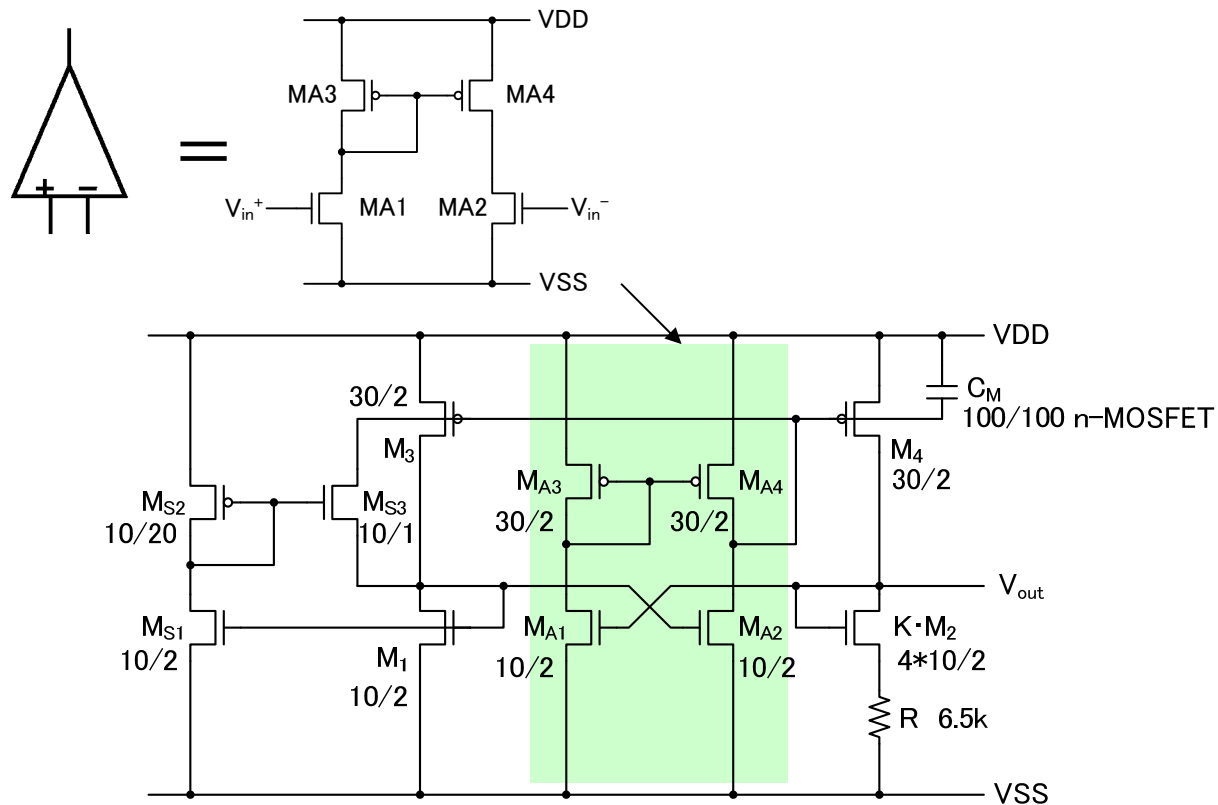
$$V_{biasp} = A_d (V_{out} - V_{biasn}) \xrightarrow{A_d \rightarrow \infty} V_{out} = V_{biasn}$$



Negative feedback control  
to maintain  $V_{biasn} = V_{out}$

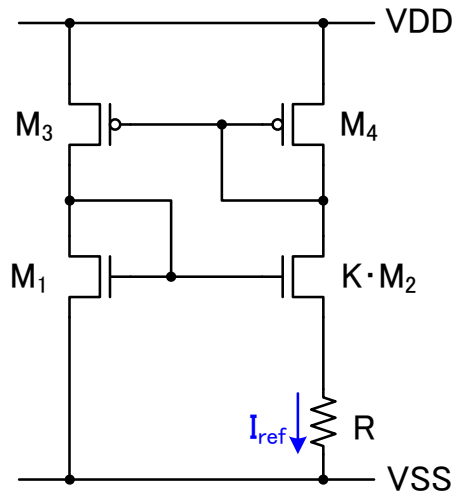
# Low-voltage BMR with the voltage regulation

BMR circuit for the short channel MOSFET



# Sub-threshold BMR for low-power circuits

Very low power consumption BMR



The circuit topology is same as the normal BMR.

$I_{DS}$ - $V_{GS}$  characteristic in the sub-threshold region.

$$I_{DS} = \frac{W}{L} I_0 \exp\left\{\frac{q(V_{GS} - V_T)}{mkT}\right\}, \quad m = 1 + \frac{C_D}{C_{OX}}$$

$$\begin{cases} V_{GS1} = m \frac{kT}{q} \ln\left(\frac{I_{ref}}{I_0} \frac{L}{W}\right) + V_{Tn} \\ V_{GS2} = m \frac{kT}{q} \ln\left(\frac{I_{ref}}{I_0} \frac{L}{K \cdot W}\right) + V_{Tn} \end{cases}$$

$$I_{ref} = \frac{1}{R} (V_{GS1} - V_{GS2})$$

$$= \frac{m kT}{R q} \ln K$$

NOTE: The very large resistance R is required.

## 9.3 Band-gap reference (BGR)

It is not easy to cancel the temperature dependence of  $R^2\beta$  in BMR shown in slide 7, because R and MOSFET are fabricated in the different stages of the CMOS process. The temperature coefficient of the reference voltage can be compensated with a pair of pn junctions.

# Temperature dependence of pn junction diode

The temperature coefficient is canceled with pn diode.

DC characteristic of pn junction ----

NOTE: Only a diffusion current is modeled in this equation. Therefore, the appropriate bias voltage have to be applied to the pn junction.

$$I = I_S \left( e^{\frac{qV_D}{kT}} - 1 \right) \cong I_S e^{\frac{qV_D}{kT}}$$

$$V_D = \frac{kT}{q} \ln\left(\frac{I}{I_S}\right)$$

$$I_S = AT^3 e^{-\frac{E_G}{kT}}$$

$I_S$ : Reverse saturation current

$k$ : Boltzmann constant (8.62E-5 eV/K)

$T$ : Absolute temperature (K)

$q$ : electron charge (1.60E-19 coulomb)

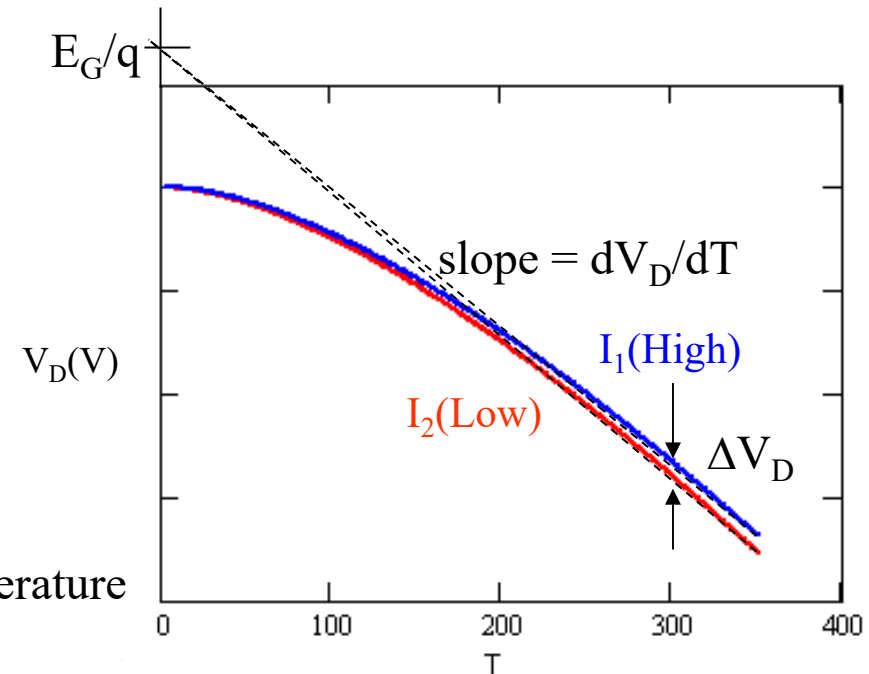
$E_G$ : Band-gap energy of Si (1.1eV)

$A$ : Constant depending on the effective density of state and impurity concentrations

# CTAT (Complementary to absolute temperature)

$$\begin{aligned}
 V_D &= \frac{kT}{q} \ln\left(\frac{I}{I_S}\right) \\
 &= \frac{kT}{q} \ln\left(\frac{I}{AT^3} e^{\frac{E_G}{kT}}\right) \\
 &= \frac{1}{q} \left(kT \ln \frac{I}{T^3} - kT \ln A + E_G\right)
 \end{aligned}$$

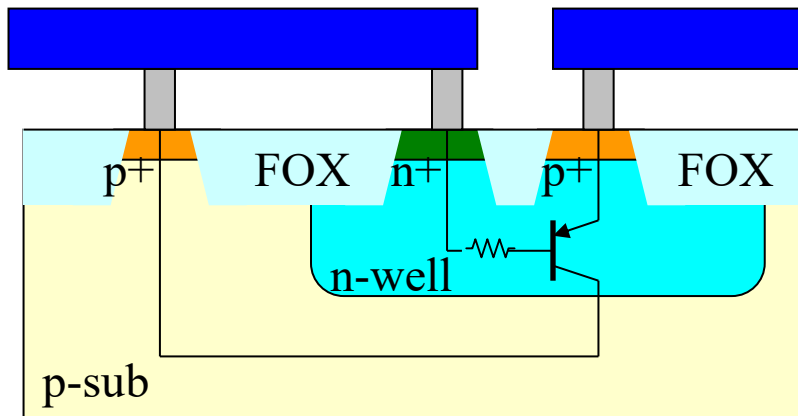
$$\frac{dV_D}{dT} \approx -\frac{k}{q} \ln A \quad \text{CTAT at room temperature}$$



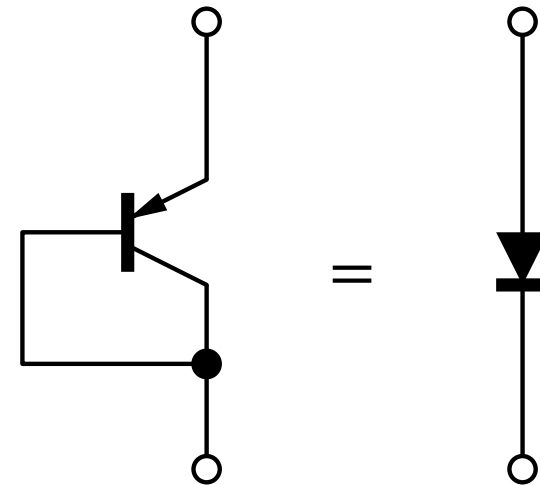
- {  $V_D$  has a negative temperature coefficient at room temperature.
- {  $\Delta V_D$  has a positive temperature coefficient at room temperature.



# Structure of the pn junction diode



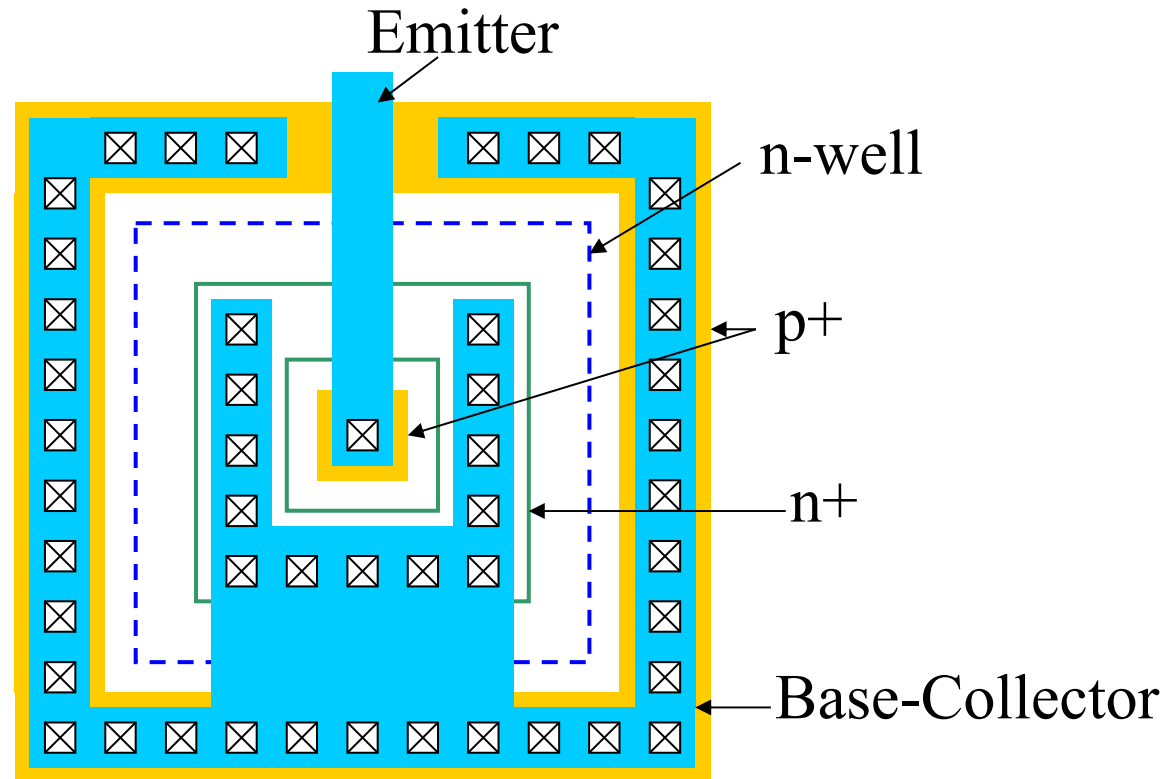
Vertical CMOS well bipolar junction transistor



Equivalent schematic

The current  $I_B$  should be limited less than 0.1mA to reduce the voltage drop in the base resistance of pnp transistor.

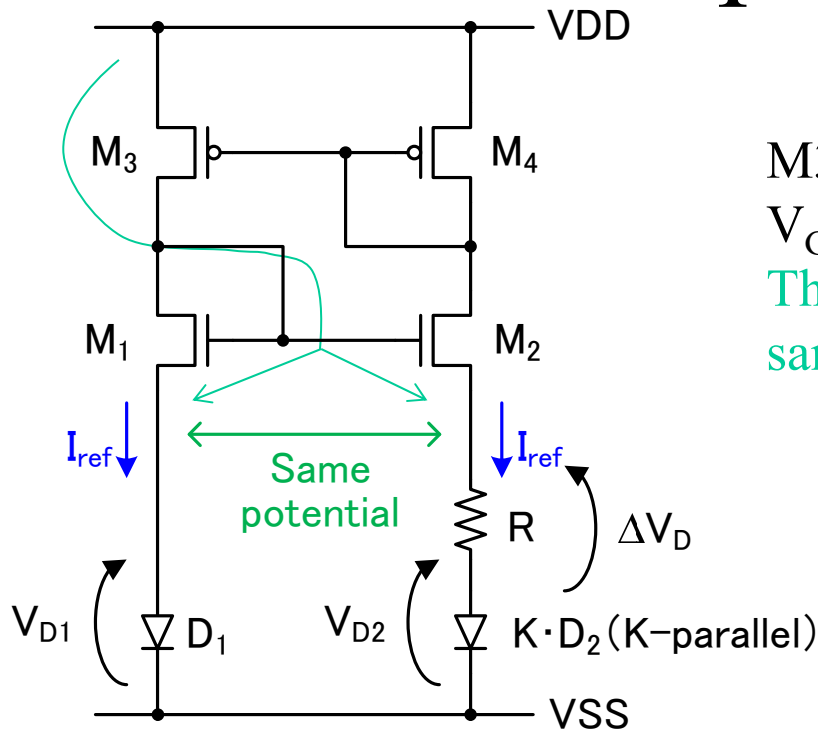
# Layout sample of the pn junction diode



Check the production tolerance of pn junction.

The standard deviation of the I-V characteristics of pn junction is rather smaller than  $V_T$  of MOSFET, but it may not be controlled by the foundry.

# PTAT (Proportional to absolute temperature)



M3, M4: Current mirror.

$V_{GS1} = V_{GS2}$  (because the  $I_{DS1} = I_{DS2}$ )

The source potential of M1 and M2 is same, then

$$V_{D1} = V_{D2} + \Delta V_D$$

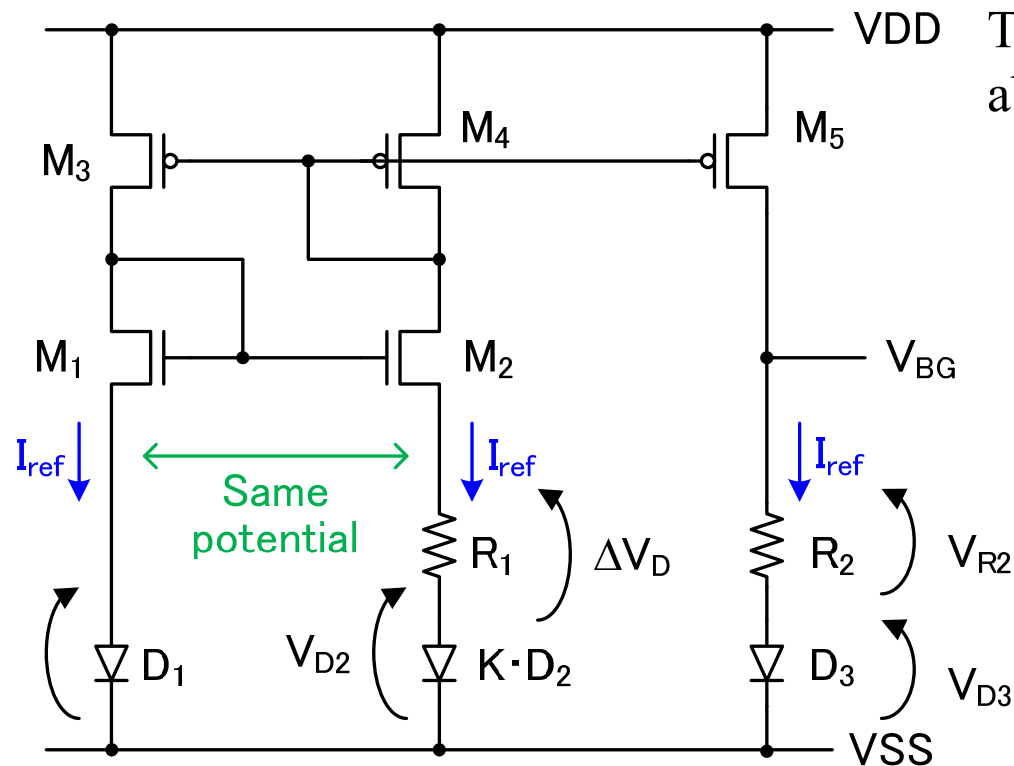
$$\begin{cases} I_{D1} = \frac{1}{K} I_{D2} \\ V_{D1} = \frac{kT}{q} \ln\left(\frac{I_{ref}}{I_S}\right) \\ V_{D2} = \frac{kT}{q} \ln\left(\frac{I_{ref}}{KI_S}\right) \end{cases}$$

(Start-up circuit is required.)

$\Delta V_D$  has a positive temperature coefficient

$$\Delta V_D = \frac{kT}{q} \left( \ln \frac{I_{ref}}{I_S} - \ln \frac{I_{ref}}{KI_S} \right) = \frac{kT}{q} \ln K$$

# BGR voltage reference



The current  $I_{ref}$  is proportional to absolute temperature (PTAT).

$$I_{ref} = \frac{\Delta V_D}{R_1} = \frac{kT}{qR_1} \ln K \quad (1)$$

$$V_{BG} = V_{D3} + R_2 \cdot I_{ref}$$

$$= V_{D3} + \frac{R_2}{R_1} \Delta V_D$$

Negative temperature coefficient      Positive temperature coefficient

# Cancelation of temperature coefficient

$$\begin{aligned}
 V_{BG} &= V_{D3} + \frac{R_2}{R_1} \Delta V_D \\
 &= \frac{kT}{q} \ln \frac{I_{ref}}{AT^3} + \frac{E_G}{q} + \frac{R_2}{R_1} \frac{kT}{q} \ln K \\
 &= \frac{kT}{q} \left( \frac{R_2}{R_1} \ln K - \ln \frac{AT^3}{I_{ref}} \right) + \frac{E_G}{q} \\
 &\quad \downarrow \\
 &\quad 0 \\
 \frac{R_2}{R_1} &= \frac{\ln \frac{AT^3}{I_{ref}}}{\ln K} \quad (2) \quad \rightarrow
 \end{aligned}$$

Note: The equation (1) is satisfied at the given temperature . You need to measure  $AT^3$  at the operating temperature of the circuit.

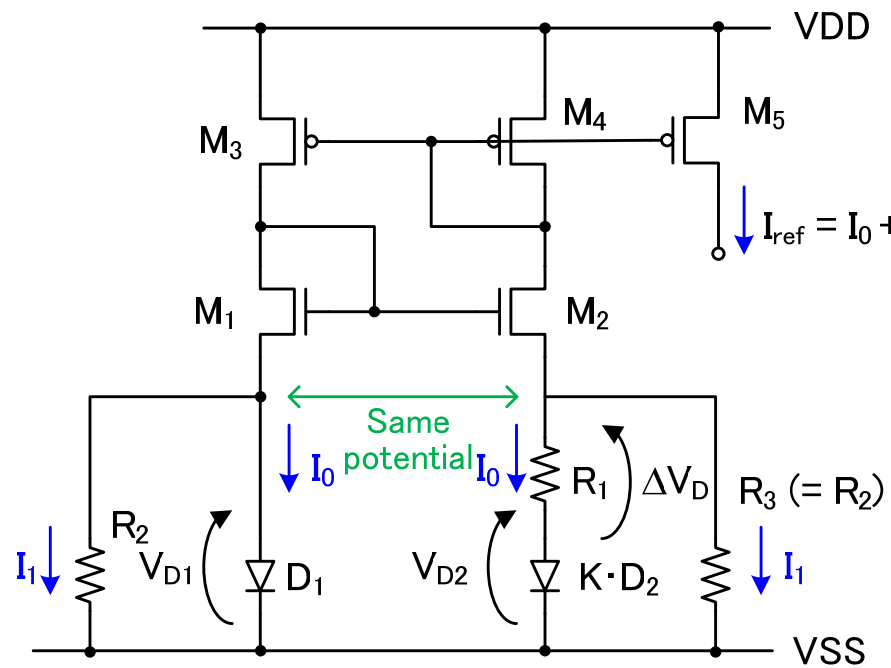
Band-gap Reference

$$V_{BG} = \frac{E_G (J)}{q(\text{coulomb})}$$



# BGR current reference

Temperature-independent current reference circuit with BGR

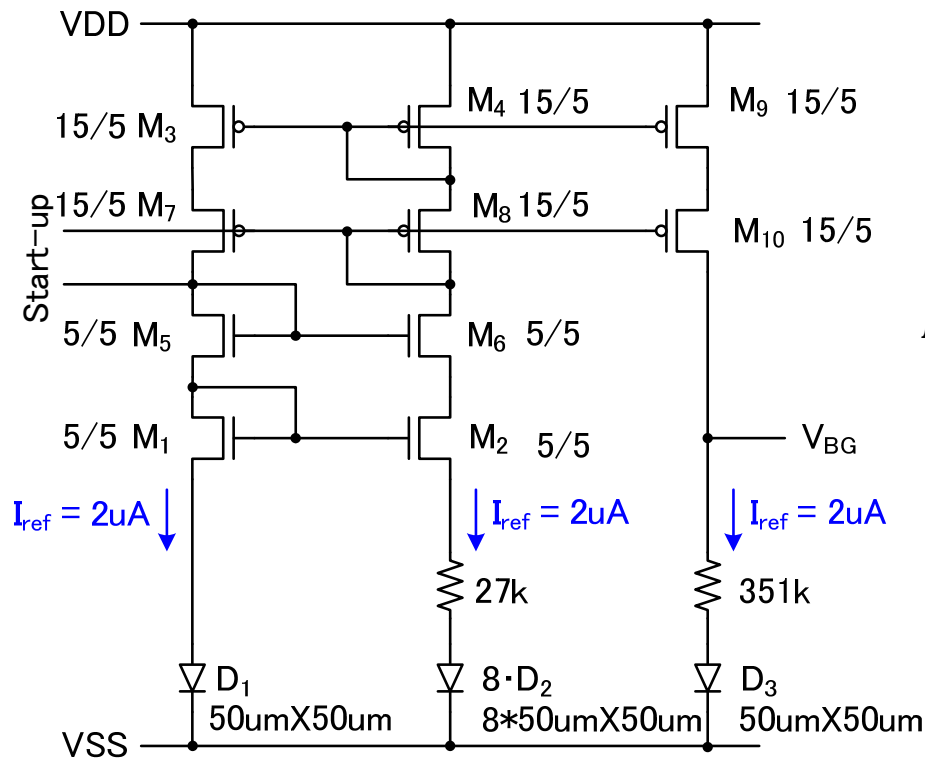


$$\begin{cases}
 I_0 = \frac{\Delta V_D}{R_1} = \frac{kT}{qR_1} \ln K \cdot \dots \cdot PTAT \\
 I_1 = \frac{V_{D1}}{R_2} = \frac{1}{qR_2} \left( -kT \ln \frac{AT^3}{I} + E_G \right)
 \end{cases}$$

$$I_0 + I_1 = \frac{kT}{q} \left( \frac{1}{R_1} \ln K - \frac{1}{R_2} \ln \frac{AT^3}{I} \right) + \frac{E_G}{qR_2}$$

$$\underbrace{\left( \frac{1}{R_1} \ln K - \frac{1}{R_2} \ln \frac{AT^3}{I} \right)}_0 = \frac{\ln \frac{AT^3}{I}}{\ln K} \cdot \frac{R_2}{R_1}$$

# Design example of cascode BGR



Say  $I_{ref} = 2\mu A$ ,  $K = 8$ ,  $W_1/L_1 = 1$

$$\Delta_{OV} = \sqrt{2I_{ref}/\beta_1} = \sqrt{2 \cdot 2\mu / (98\mu \cdot 1)} = 0.20V$$

From Eq.(1) shown in the slide 20,

$$R = \frac{1}{I_{ref}} \frac{kT}{q} \ln(K) = \frac{1.380 \cdot 10^{-23} \cdot 300}{2\mu \cdot 1.602 \cdot 10^{-19}} \ln 8 = 27k\Omega$$

From the simulation result for 50um-square diode.

$$I_s = 3.45 \cdot 10^{-13}$$

$$A = \frac{I_s}{T^3} e^{\frac{E_G}{kT}} = \frac{3.45 \cdot 10^{-13}}{300^3} e^{\frac{1.1eV}{8.62 \cdot 10^{-5} \cdot 300}} = 0.038$$

From Eq.(2) shown in the slide 21,  $L = \frac{\ln\left(\frac{AT^3}{I_{ref}}\right)}{\ln(K)} = \frac{\ln\left(\frac{0.038 \cdot 300^3}{2\mu}\right)}{\ln(8)} = 13$  24