8. Bias circuits

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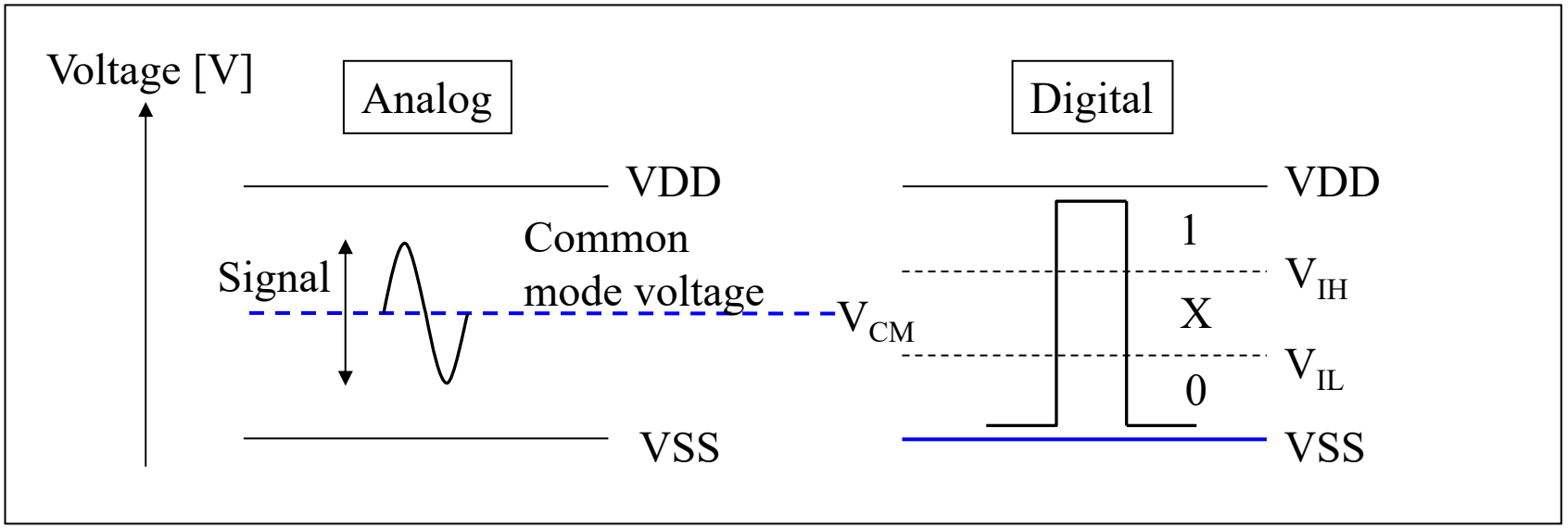
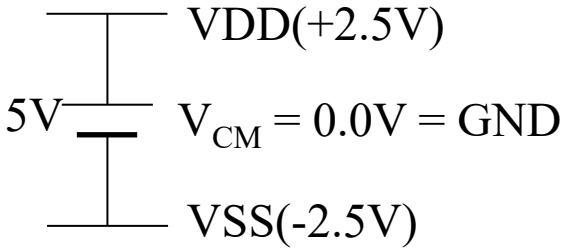
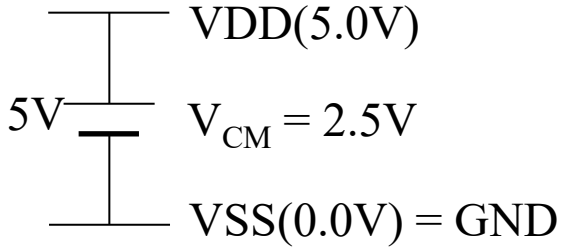
8.1 Current Mirror

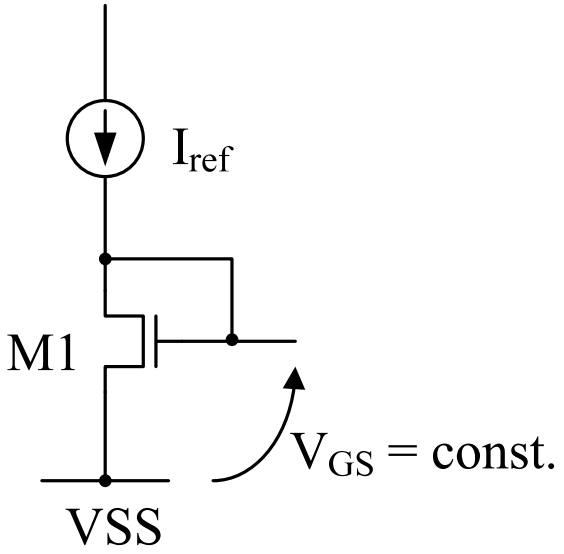
Electrical potential of the rails







Constant voltage circuit



$$\begin{cases} V_{DS} = V_{GS} \\ V_{DS} \geq V_{GS} - V_{Tn} = \Delta_{OV} \end{cases}$$

Therefore, M1 is driven in the saturation region. This circuit can output the voltage V_{GS} controlled by I_{ref}.

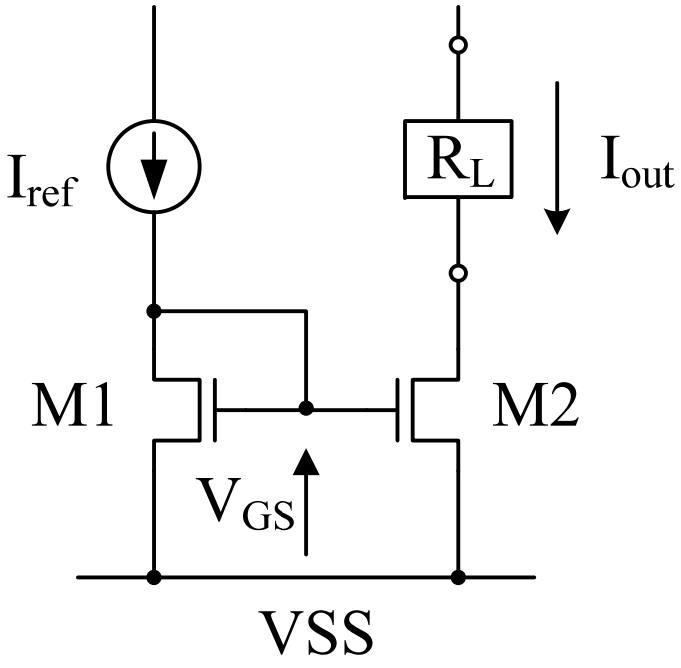
In the saturation region

$$I_D = I_{ref} = \frac{\beta_1}{2}(V_{GS} - V_{Tn})^2$$

I_D = const.	$\rightarrow V_{GS}$ = const.
V_{GS} = const.	$\rightarrow I_D$ = const.

$$V_{GS}(I_{ref}) = V_{Tn} + \sqrt{\frac{2I_{ref}}{\beta_n}} = V_{Tn} + \Delta_{OV}$$ (Δ_{OV}: Overdrive voltage)

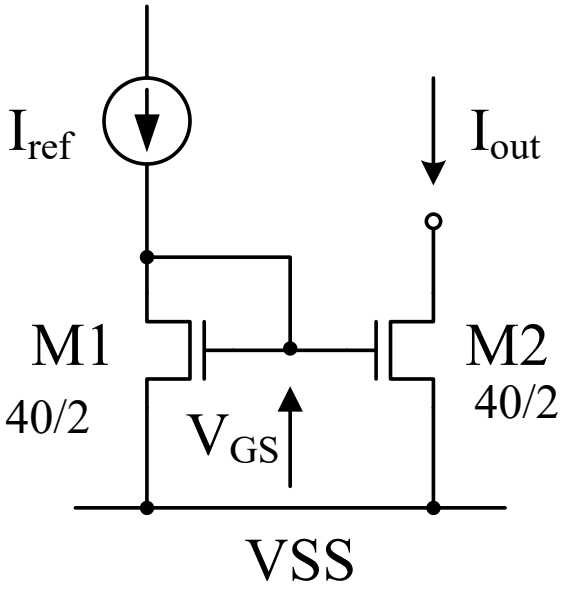
Current mirror

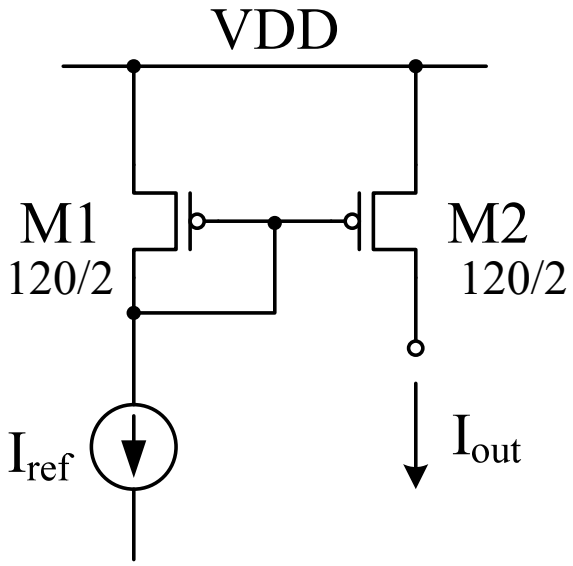


$$\begin{cases} I_{out} = \dfrac{\beta_2}{2}(V_{GS} - V_{Tn})^2 \\ I_{ref} = \dfrac{\beta_1}{2}(V_{GS} - V_{Tn})^2 \end{cases}$$

$$\therefore I_{out} = \frac{\beta_2}{\beta_1} I_{ref} = \frac{(\frac{W}{L})_2}{(\frac{W}{L})_1} I_{ref}$$

Sink and source of the current mirror



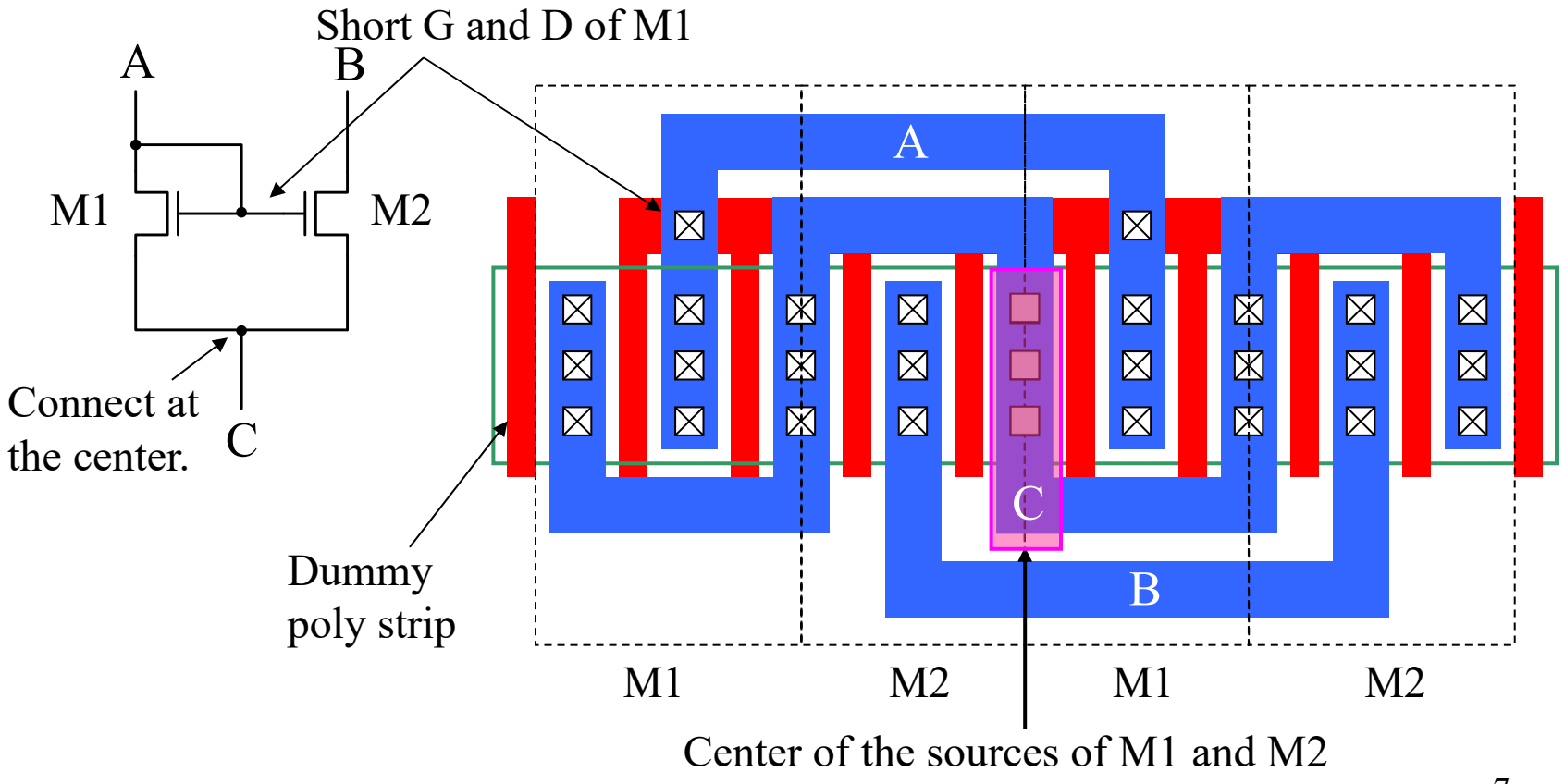


Current Sink

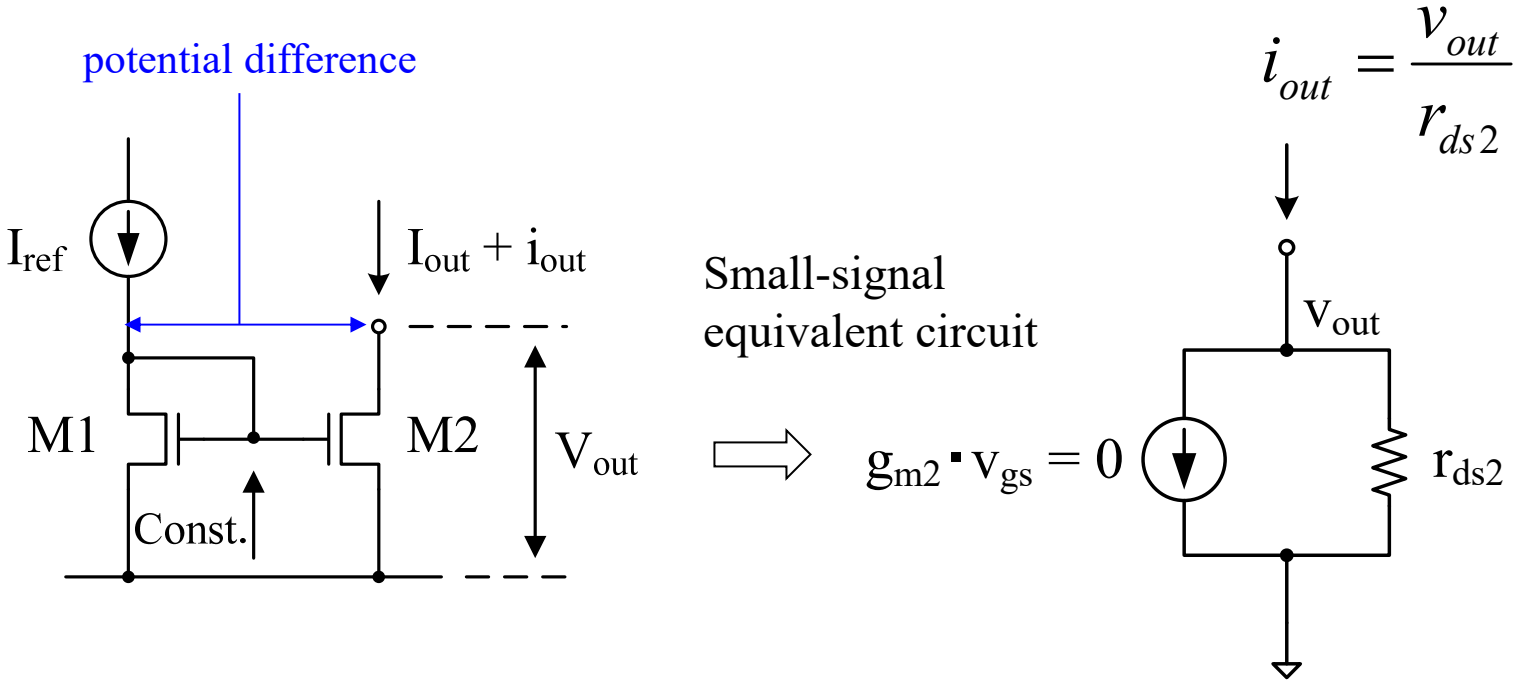
$$I_{out} = \frac{(\frac{W}{L})_2}{(\frac{W}{L})_1} I_{ref}$$

Current Source

Layout sample of the current mirror



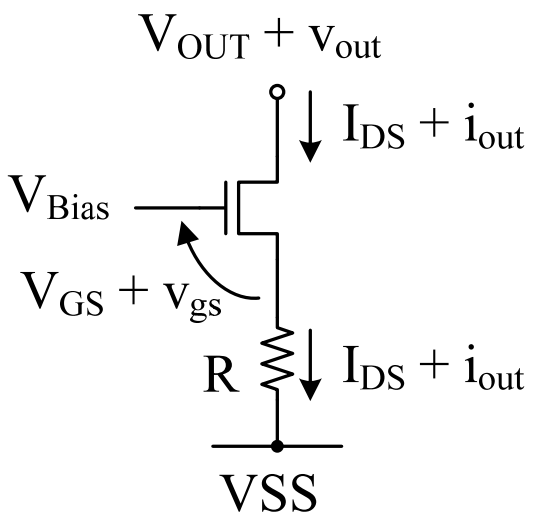
Deviation from the ideal characteristics



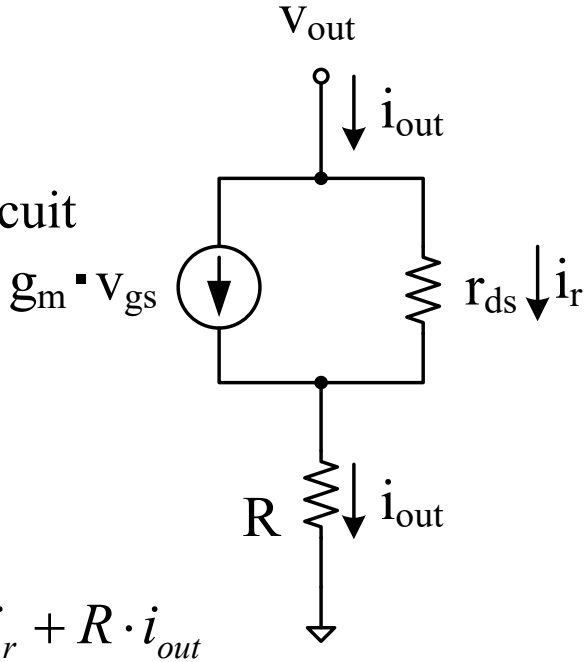
The channel resistance of M2 is not infinite, therefore, M2 cannot work as an ideal current source. The higher drain resistance of M2 is preferable to improve the characteristic of the current source.

Cascaded Triode (Cascode circuit)

Gate-common MOSFET acts as a trans-impedance amplifier.



Small-signal equivalent circuit

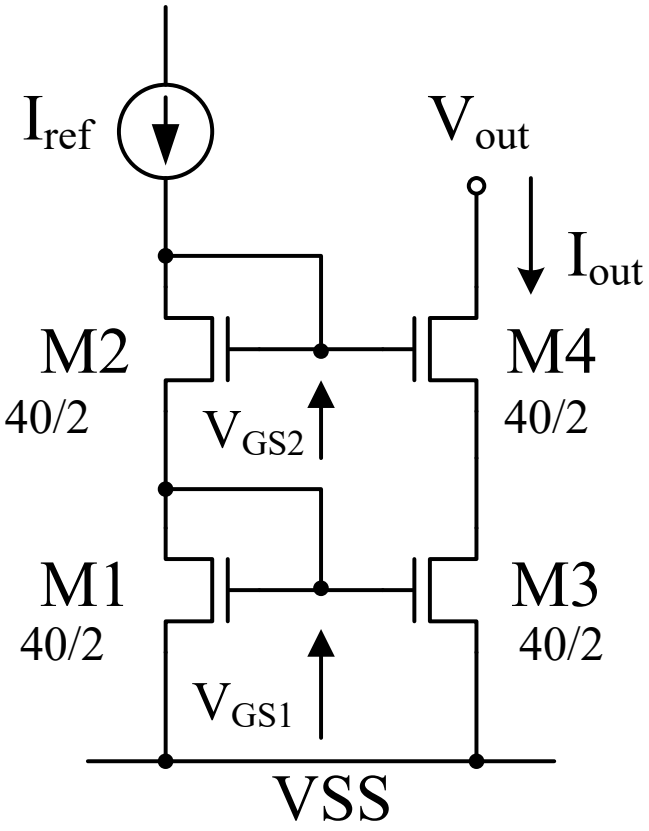


$$i_{out} = g_m \cdot v_{gs} + i_r$$
$$= g_m \cdot (-R \cdot i_{out}) + i_r$$
$$i_r = (1 + g_m R) \cdot i_{out}$$

$$v_{out} = r_{ds} \cdot i_r + R \cdot i_{out}$$
$$= r_{ds} \cdot (1 + g_m R) \cdot i_{out} + R \cdot i_{out}$$
$$\approx g_m r_{ds} R \cdot i_{out}$$

The output resistance is amplified to 10~1000times.

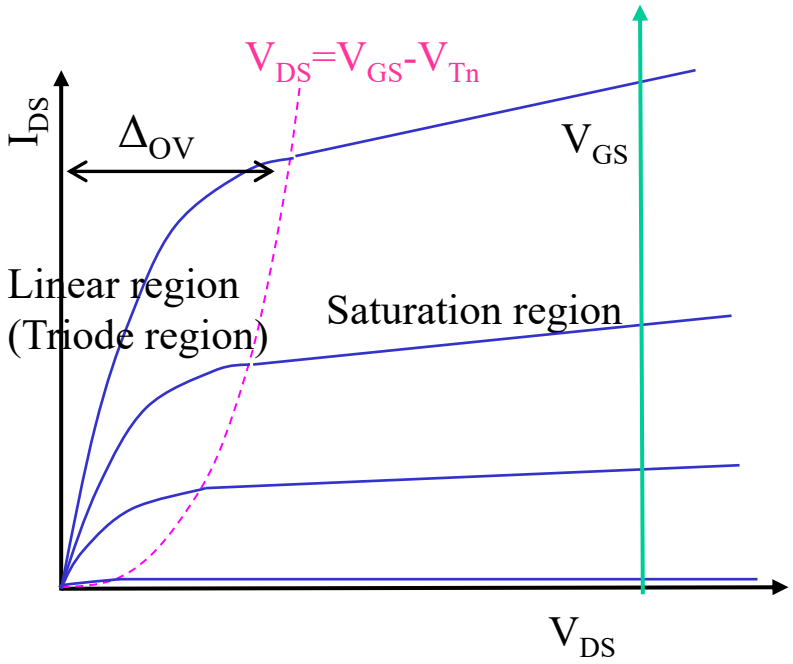
Cascode current mirror

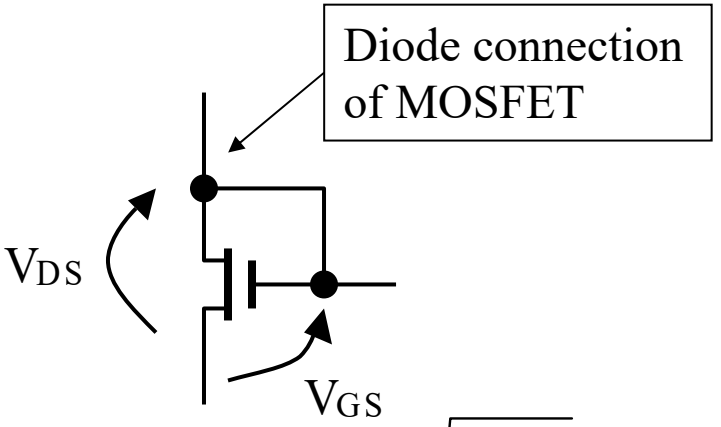


$$i_{out} = \frac{v_{out}}{(g_{m4} \cdot r_{ds4}) r_{ds3}}$$

i_{out}, that is, the variation of I_{out} is reduced by the large output resistance.

Bias condition of MOSFET in current mirror circuits





$$\Delta_{OV} = V_{GS} - V_{Tn} = \sqrt{\frac{2I_{DS}}{\beta_n}}$$

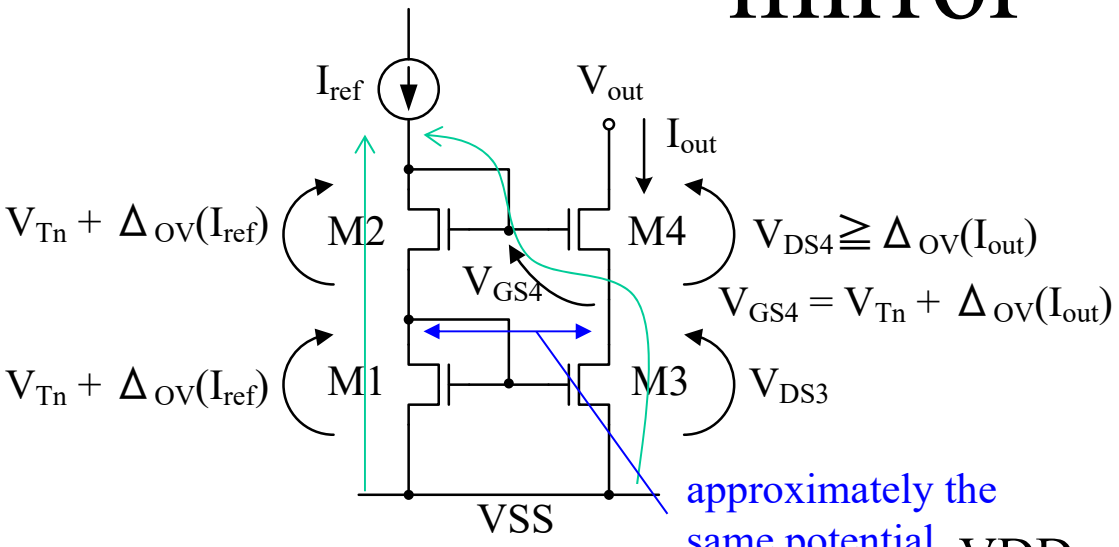
$$If \quad V_{GS} = V_{DS},$$

$$V_{DS} = V_{Tn} + \Delta_{OV}(I_{DS})$$

For diode connection: $V_{DS} = V_{Tn} + \Delta_{OV}(I_{DS})$

For constant V_{GS} $V_{DS} \geq \Delta_{OV}(I_{DS})$

Output voltage range of the current mirror

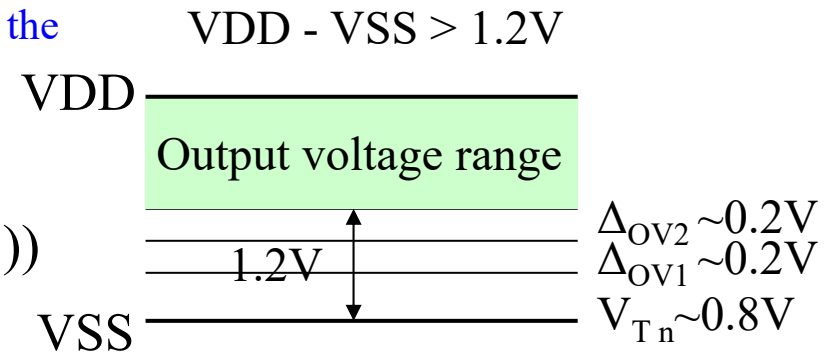


$$V_{GS1} + V_{GS2} = V_{DS3} + V_{GS4}$$

$$2(V_{Tn} + \Delta_{OV}(I_{ref})) = V_{DS3} + (V_{Tn} + \Delta_{OV}(I_{out}))$$

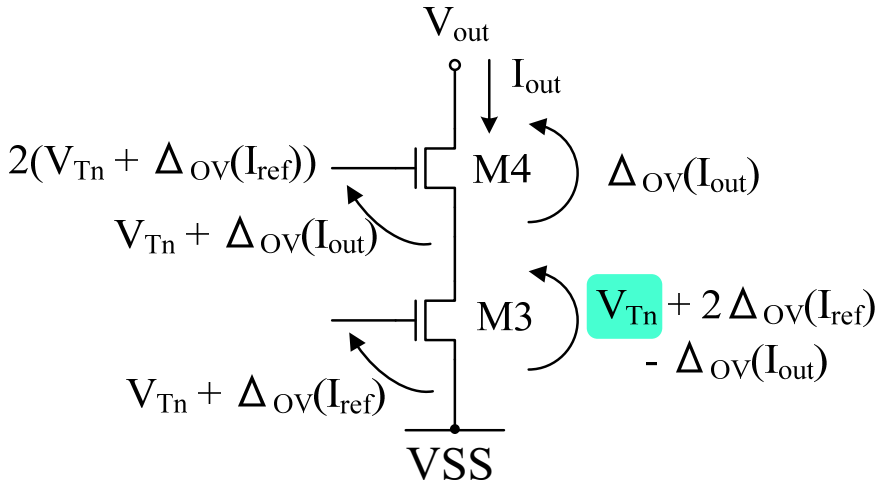
$$V_{DS3} = V_{Tn} + 2\Delta_{OV}(I_{ref}) - \Delta_{OV}(I_{out})$$

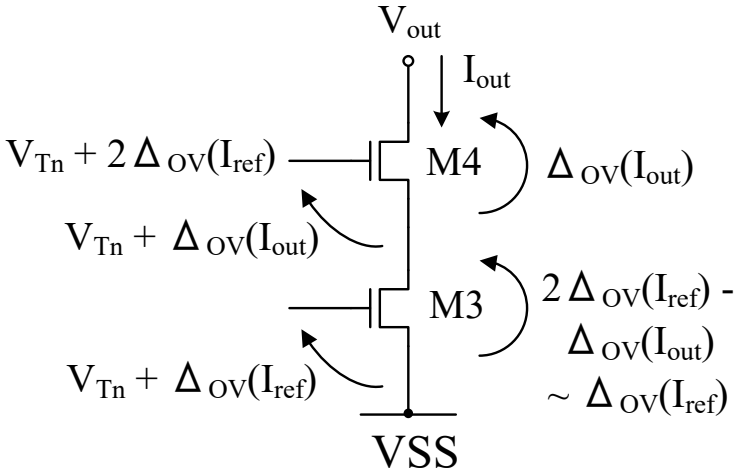
$$V_{out} = V_{DS3} + V_{DS4} \geq V_{Tn} + 2\Delta_{OV}(I_{ref})$$



Wide-swing cascode current mirror (1)

When the MOSFET M3 can work in the saturation region: $V_{DS} > \Delta_{OV}$, the lower limit of output voltage can be reduced to $2\Delta_{OV}$.





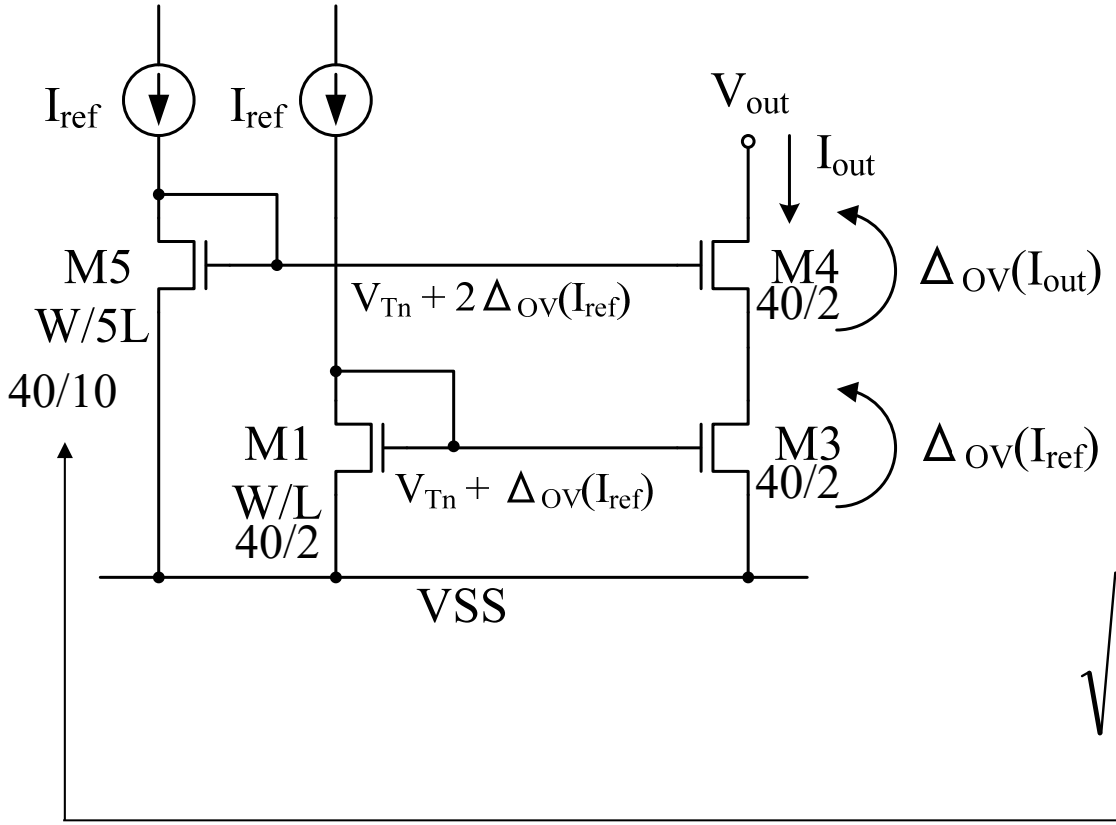
The gate voltage of M4 (= $2V_{Tn}+2\Delta_{OV}$) is over-biased to drive M3 in the saturation region.

⇒

The gate voltage of M4 can be lowered to $V_{Tn}+2\Delta_{OV}$.

Wide-swing cascode current mirror (2)

(Do not use this circuit)



$$V_{GS5} = V_{Tn} + \sqrt{\frac{2I_{ref}}{\beta_5}}$$

$$= V_{Tn} + 2\Delta_{OV}(I_{ref})$$

$$= V_{Tn} + 2\sqrt{\frac{2I_{ref}}{\beta_1}}$$

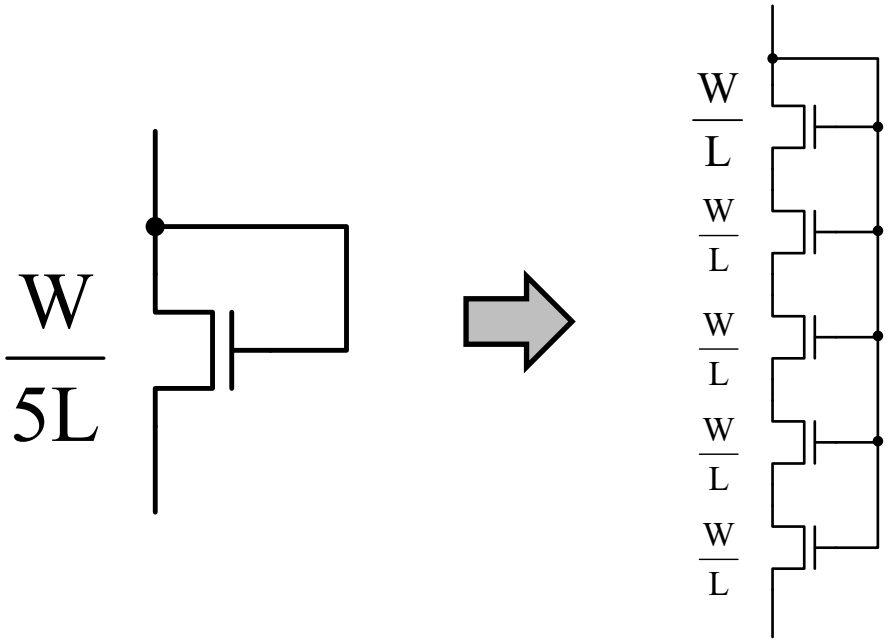
$$\sqrt{\frac{2I_{ref}}{\beta_5}} = 2\sqrt{\frac{2I_{ref}}{\beta_1}}$$

$$\therefore \beta_5 = \frac{\beta_1}{4}$$

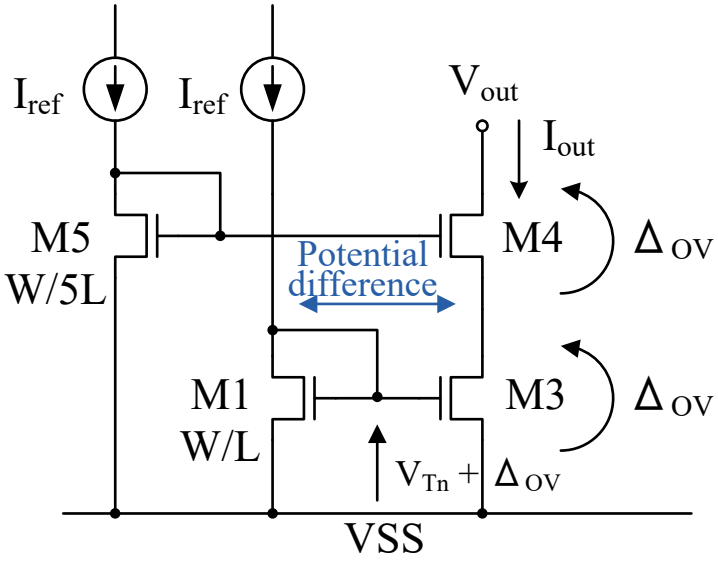
In consideration of a bias margin for the M3 saturation, the size of M5 is practically set by W/5L.

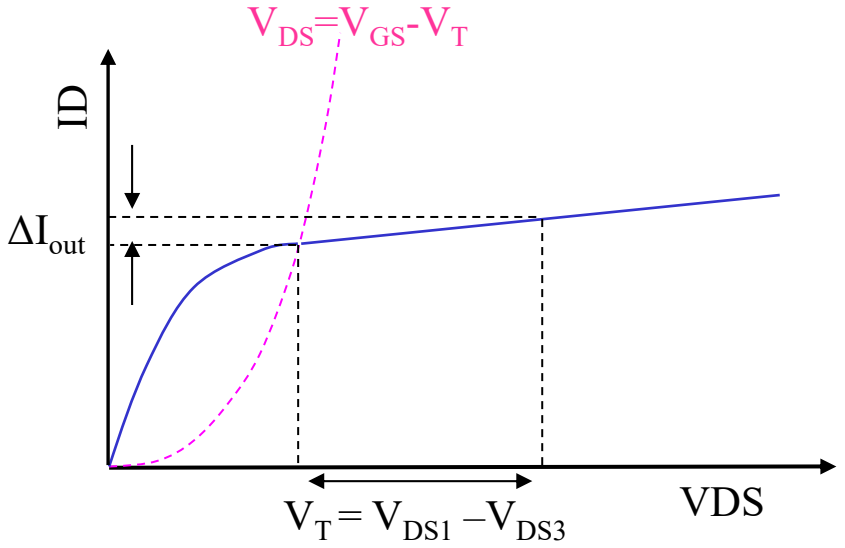
Layout method of long channel MOSFETs

The short channel effect is avoided by the series connection of W/L MOSFETs.



Current error of the wide swing cascode current mirror



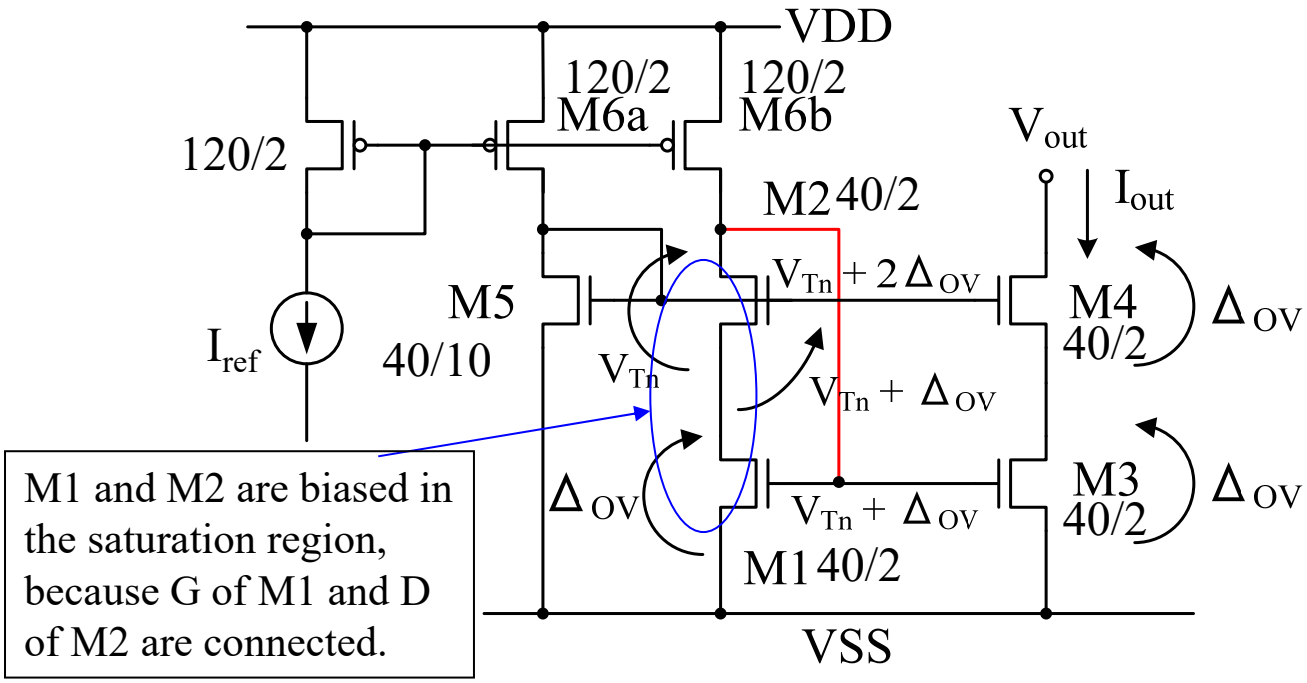


The large L of M1 and M3 can improve the saturation characteristic of the MOSFETs, but the improvement is insufficient.

The current error ΔI_{out} occurs by the difference of V_{DS1} and V_{DS3}.

※ The problem is remarkable in the short channel MOSFETs.

Practical cascode current mirror



$$V_{DS1} = V_{GS5} - V_{GS2}$$

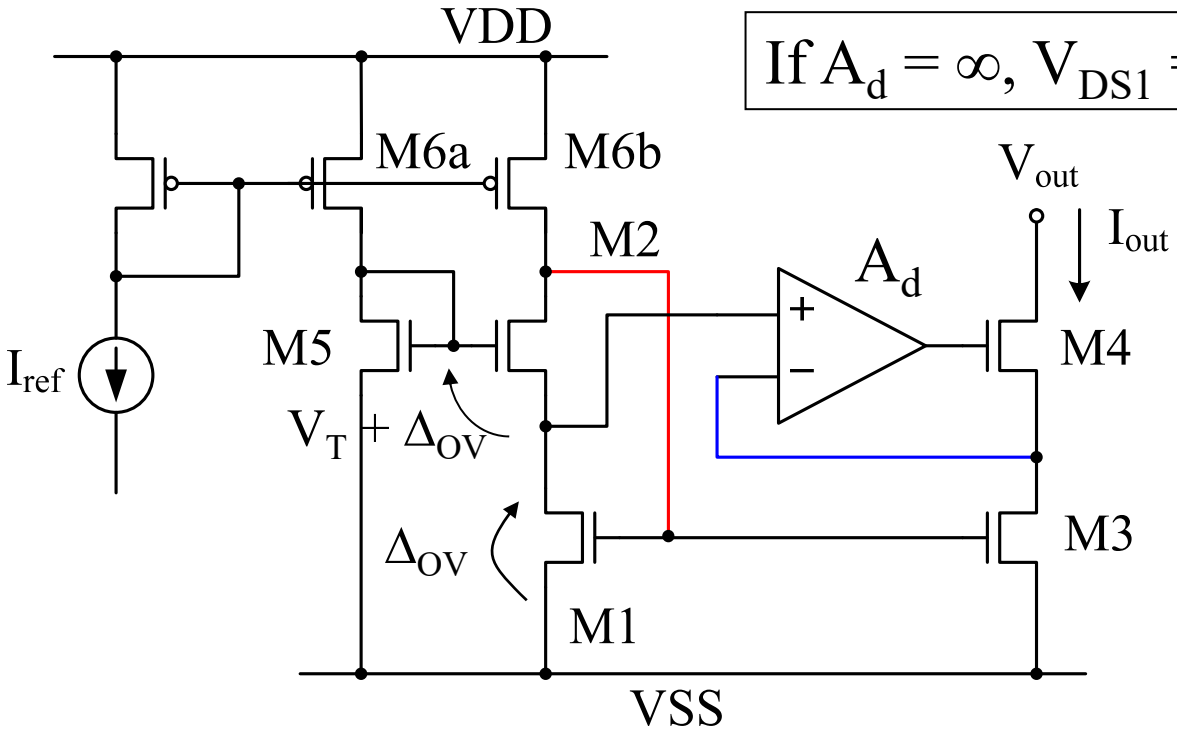
$$= V_{Tn} + 2\Delta_{OV}(I_{ref}) - (V_{Tn} + \Delta_{OV}(I_{ref}))$$

$$= \Delta_{OV}(I_{ref}) \fallingdotseq \Delta_{OV}(I_{out}) = V_{DS3}$$

If $I_{ref} = I_{out}$, $V_{DS1} \fallingdotseq V_{DS3}$ for the minimum voltage of V_{DS3}

Drain regulated current mirror

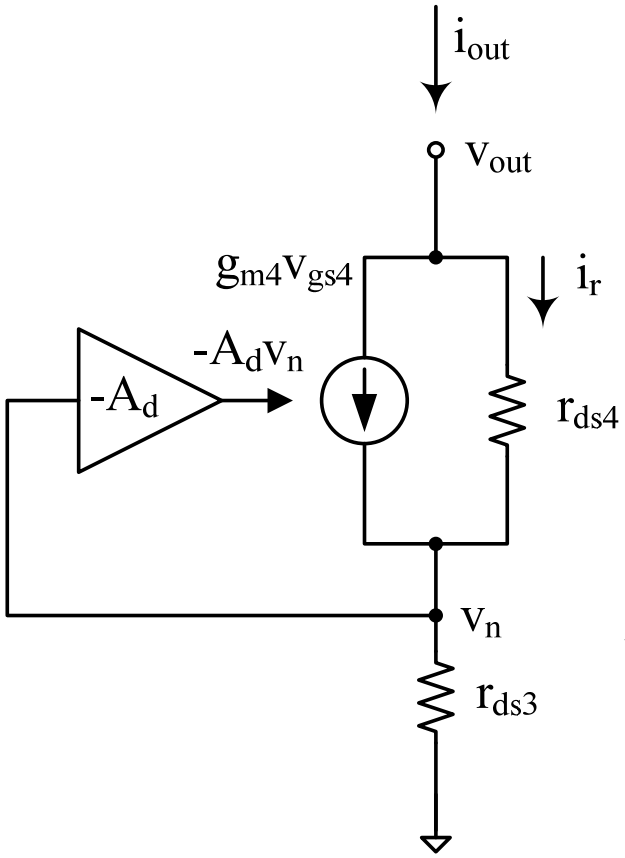
The highly precise circuit with the NFB (Negative Feedback) loop. The drain of M1 and M3 is regulated to the same potential.



If $A_d = \infty$, $V_{DS1} = V_{DS3}$

I_{DS4} is kept a constant value by the NFB control of M4. The output resistance is $\sim(A_d + 1)(g_{m4}r_{ds4}r_{ds3})$.

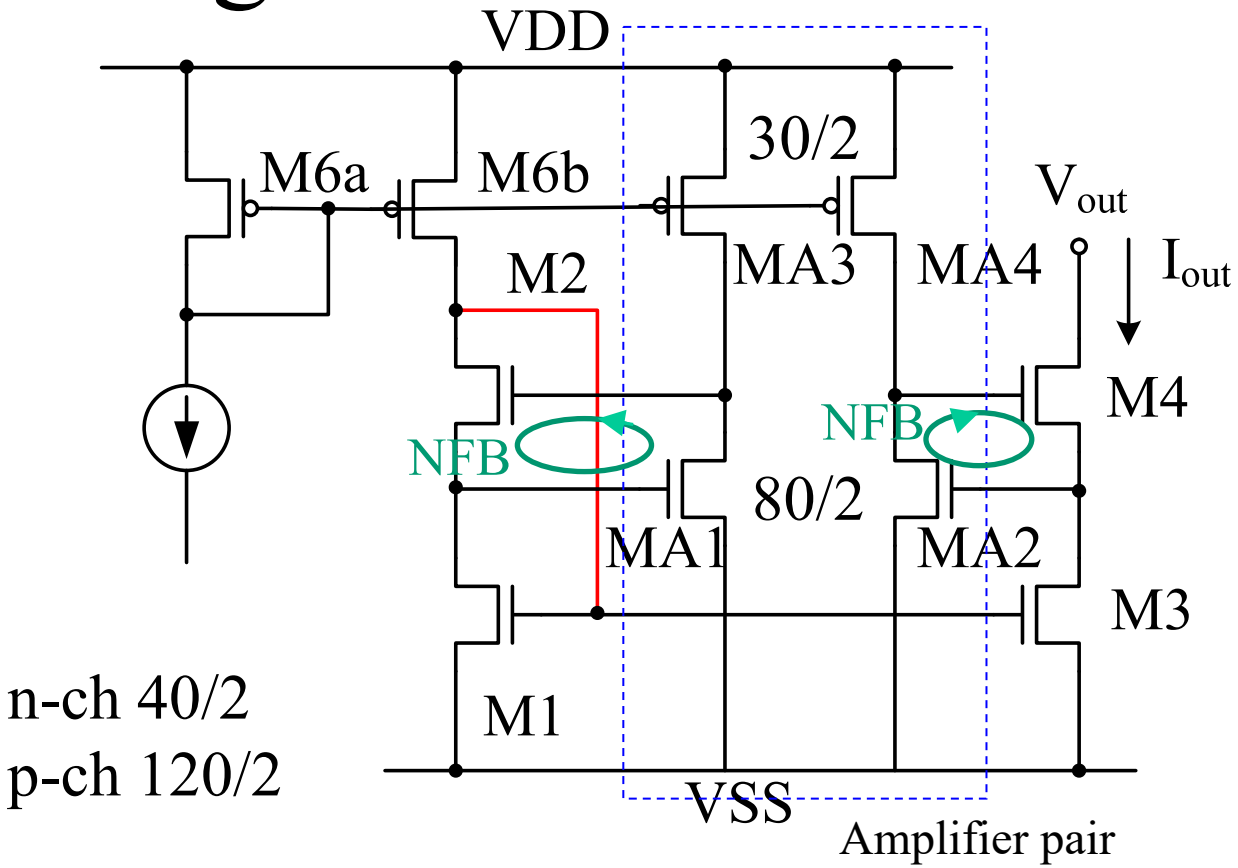
Analysis of the drain regulated circuit



$$i_{out} = g_{m4}v_{gs4} + i_r$$
$$v_{gs4} = -A_d v_n - v_n$$
$$v_n = r_{ds3} i_{out}$$
$$v_{out} = r_{ds3} i_{out} + r_{ds4} i_r$$

$$r_{out} = \frac{v_{out}}{i_{out}}$$
$$= r_{ds4} + r_{ds3} + (A_d + 1) g_{m4} r_{ds4} r_{ds3}$$

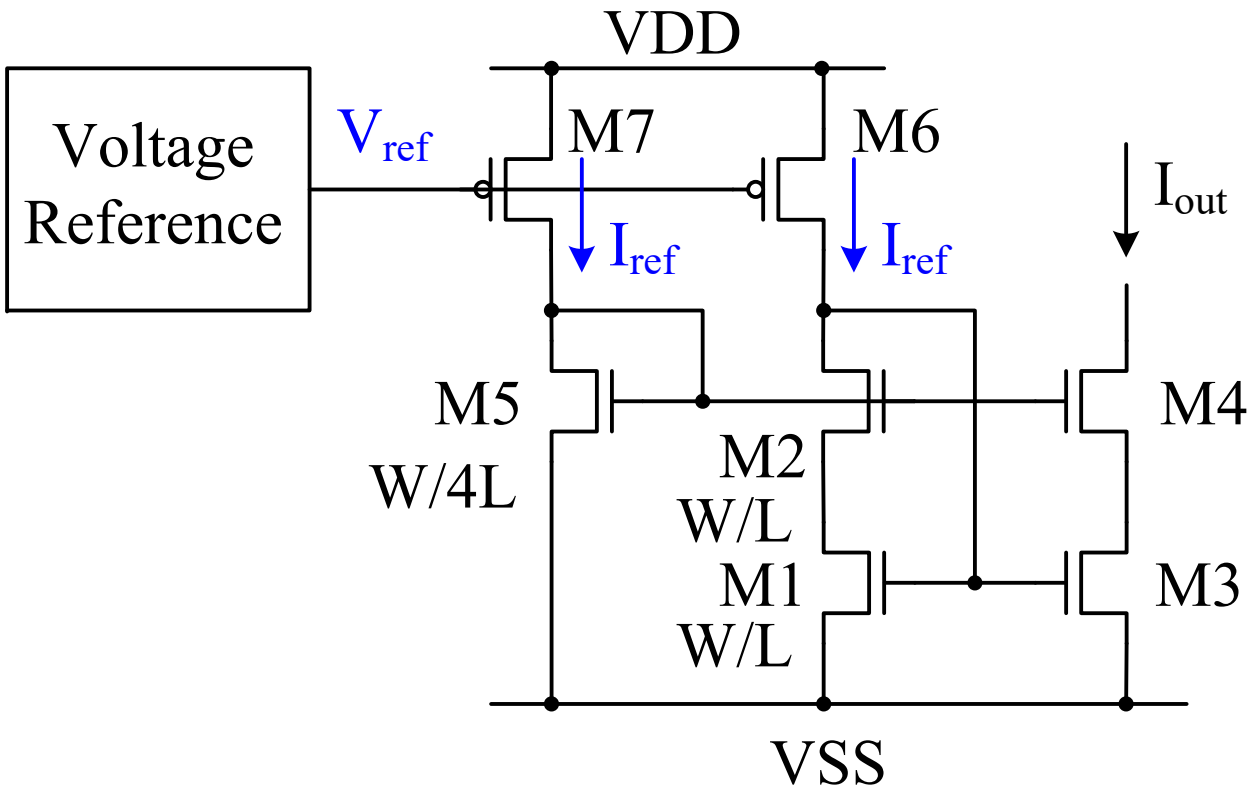
Design sample of the practical regulated drain current mirror



NOTE: The differential amplifier is displaced by an amplifier pair. Do not use this circuit as it is, because M6a and M6b are not regulated.

8.2 Bias circuits

Cascode current mirror with a voltage reference



Bias circuit based on the cascode current mirror