7. MOSFET models

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7.1 Feature of MOSFET models

SPICE models of MOSFET

Model name	Feature
Level 1	Basic physical model（L > 10um）
Level 3	Basic semi-empirical fitting model (L > 1um), Short-channel effect
BSIM3v3	Berkeley Short-channel IGFET Model, L > 130nm
BSIM4	L < 90nm, for high frequency operation
EKV	Enz-Krummenacher-Vittoz, High precision, Sub-threshold region
HiSIM	Hiroshima-Univ. STARC IGFET Model, L < 90nm, for high frequency operation

Reference of BSIM4： http://www-device.eecs.berkeley.edu

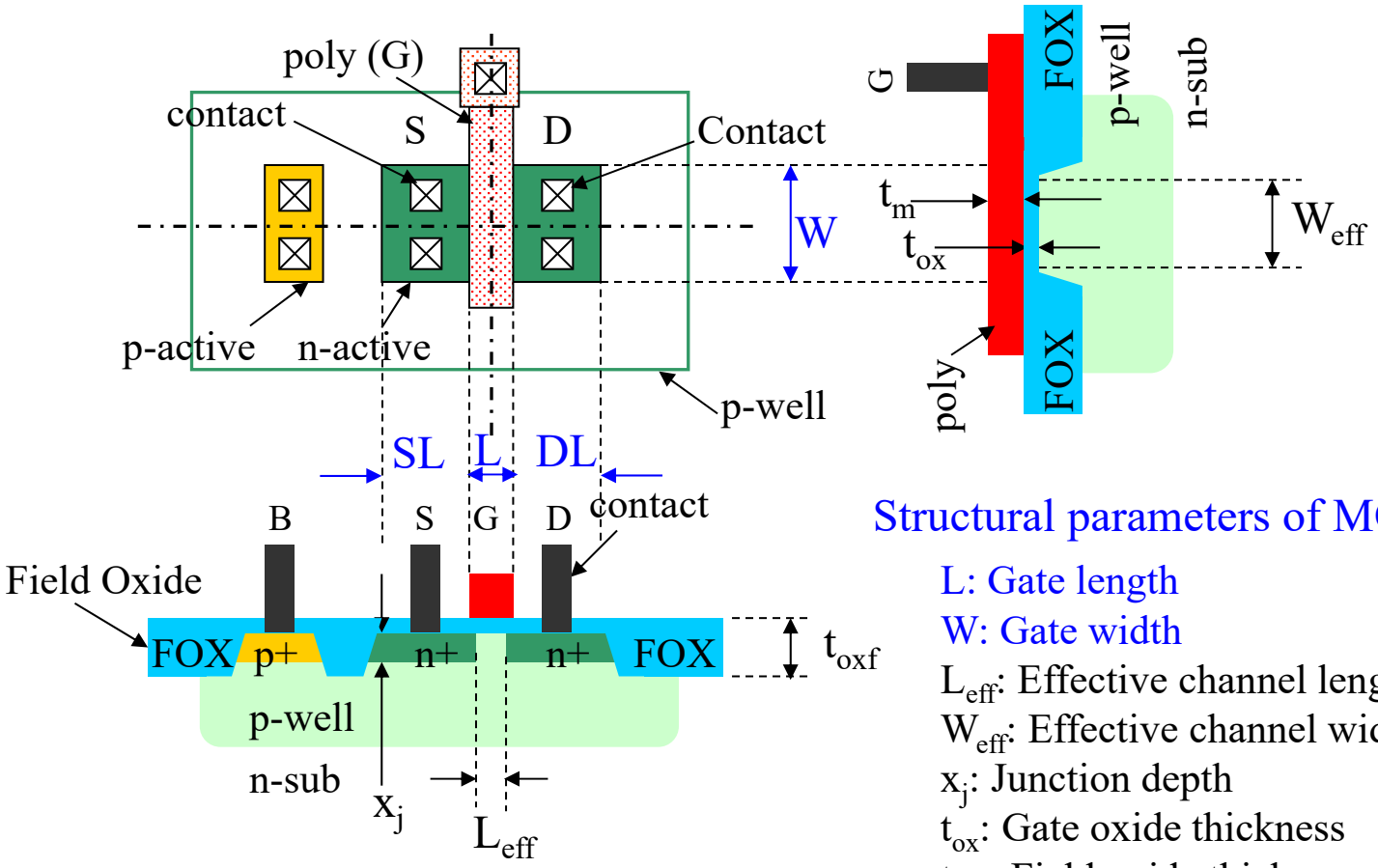
Model number

Model	HSPICE, SmartSpice	Berkeley SPICE	LTspice
Level3	3	3	3
BSIM3	49/53	8	8
BSIM4	54	14	14
BSIMSOI3	57	10	9
EPFL-EKV	55		12
HiSIMHV1.2			73

```
.model model_name NMOS/PMOS   Level=54
+ vto=0.5
+ kp=33E-6
+ .....
```

model # (The assignment of the model number depends on the circuit simulator.)

Dimensional parameters of MOSFET



Structural parameters of MOSFET

L: Gate length

W: Gate width

L_{eff}: Effective channel length

W_{eff}: Effective channel width

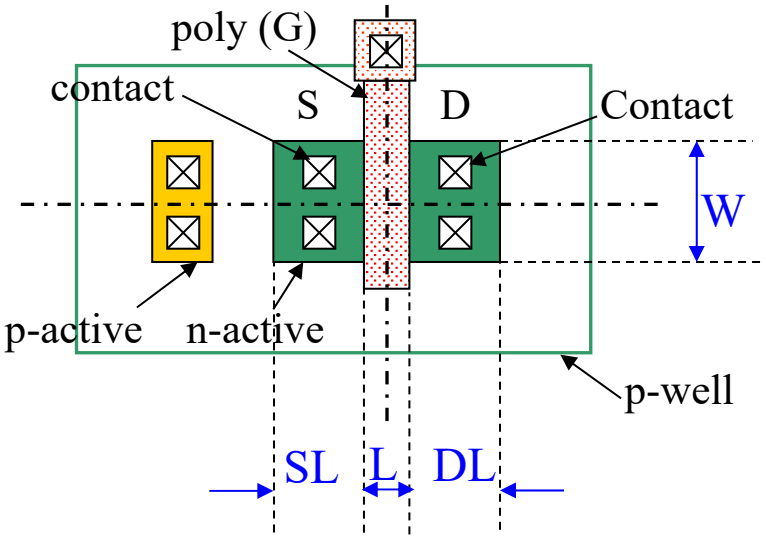
x_j: Junction depth

t_{ox}: Gate oxide thickness

t_{oxf}: Field oxide thickness

t_m: poly-Si thickness

Configurable parameters in circuit design



Spice model parameters of MOSFET

- L: Gate length
- W: Gate width
- AD: Drain area = DL·W
- AS: Source area = SL·W
- PD: Perimeter of drain = 2DL + W
- PS: Perimeter of source = 2SL + W

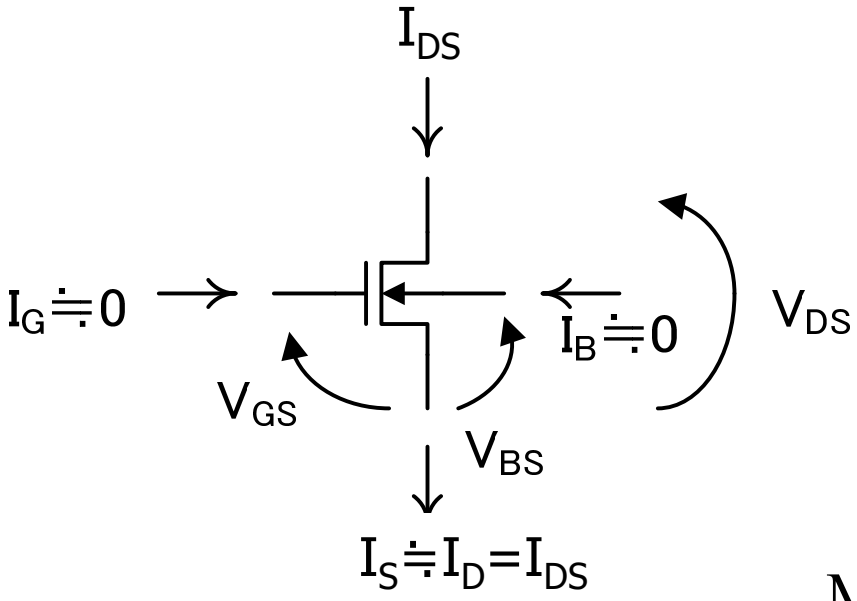
Determination of L and W

- Analog circuit: Several times larger L than minimum L
  - The production tolerance and mismatch are improved by using larger L.
  - The channel noise in MOSFET is suppressed by using larger L*W.
  - The operating frequency range is decreased by using larger L. (Disadvantage)
  - Very large W/L or M is required for current drive strength of MOSFET. (Disadvantage)

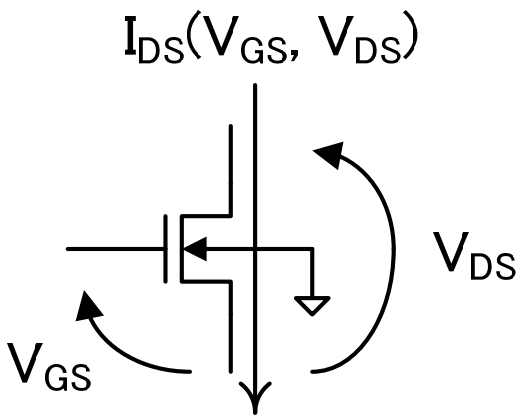
- Logic circuits: Minimum L
  - The DC transfer characteristic of the logic gate designed only in W/L.
  - The small L achieves a small circuit area.
  - The small L achieves a short delay time.

7.2 DC characteristics of long channel MOSFET

Variables of DC characteristics



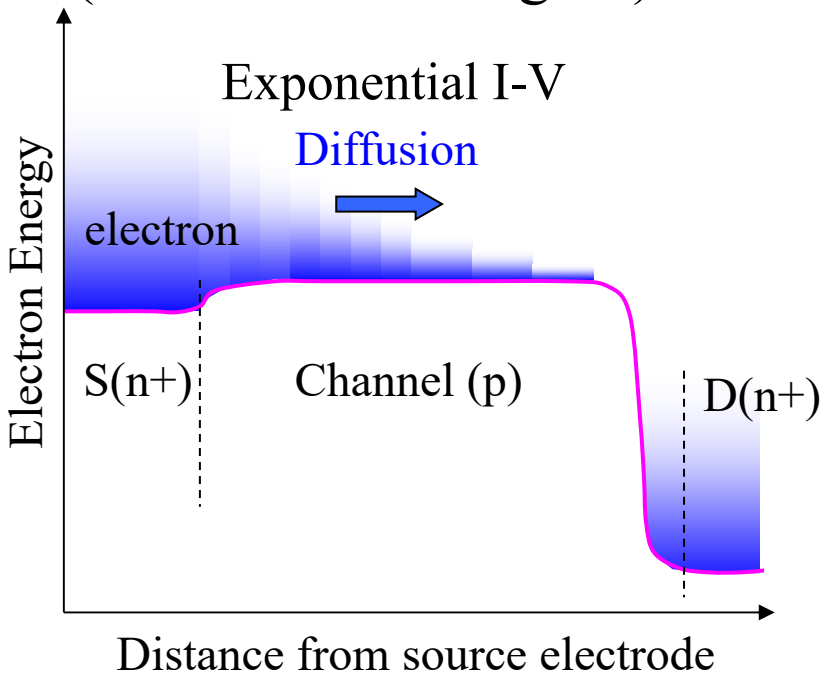
If $V_{BS} = 0V$,



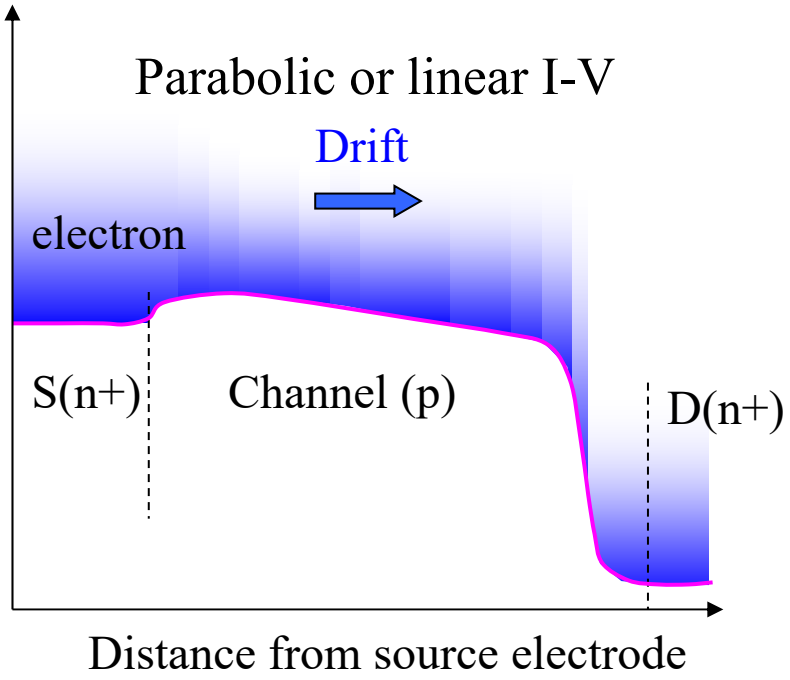
Main variables of the function I_{DS} are V_{DS} and V_{GS}.

Carrier transport mechanism in MOSFET

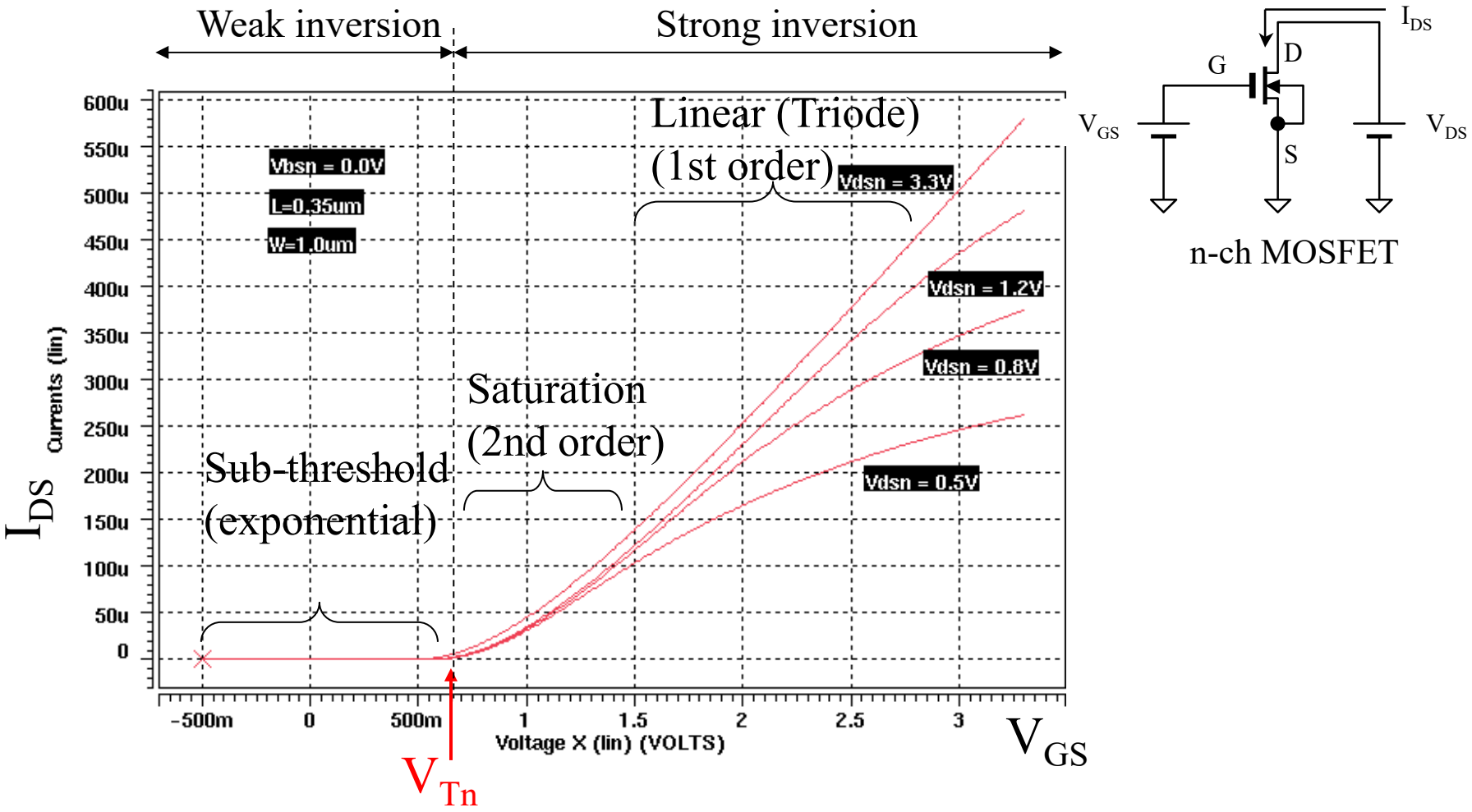
Weak inversion
(Sub-threshold region)



Strong inversion
(Linear and Saturation region)



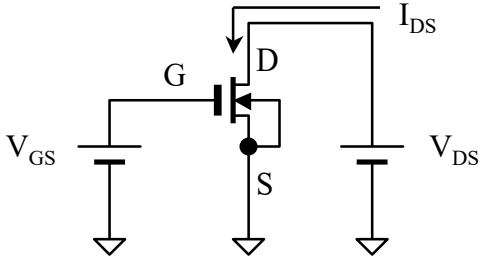
V_{GS}-I_{DS} Characteristic



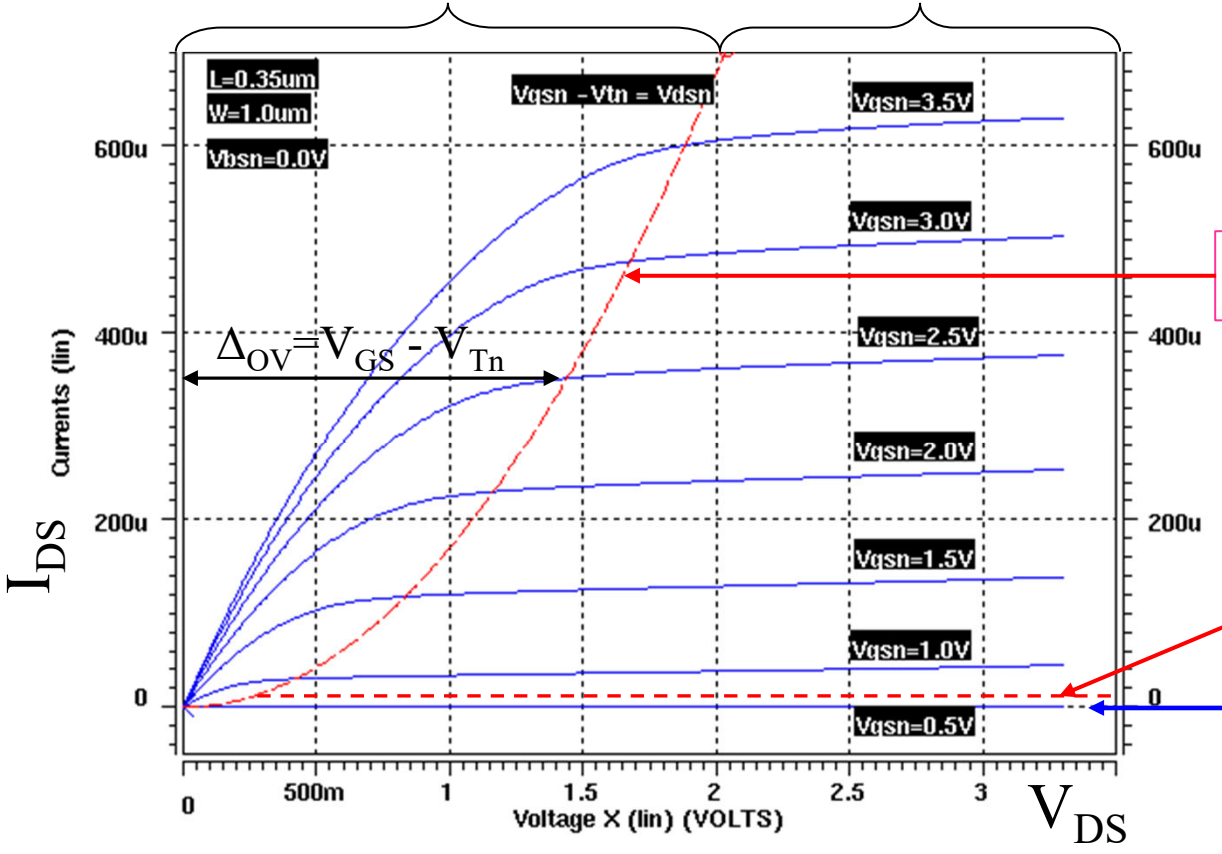
V_{DS}-I_{DS} Characteristic

$V_{DS} \le V_{GS} - V_{Tn}$ Linear (2nd order)

$V_{DS} \ge V_{GS} - V_{Tn}$ Saturation (constant)



n-ch MOSFET



$V_{DS} = V_{GS} - V_{Tn}$

$V_{GS} = V_{Tn}$

Sub-threshold

Model equation in linear region

Gradual Channel Approximation

$$I_{DS} = \frac{W_n}{L_n}\mu_n C_{OX}\{(V_{GS} - V_{Tn})\cdot V_{DS} - \frac{1}{2}V_{DS}^2\}$$

$$= \beta_n\{(V_{GS} - V_{Tn})\cdot V_{DS} - \frac{1}{2}V_{DS}^2\}$$

1st order for V_{GS} 2nd order for V_{DS}

μ_n : Electron mobility [m^2/Vs]

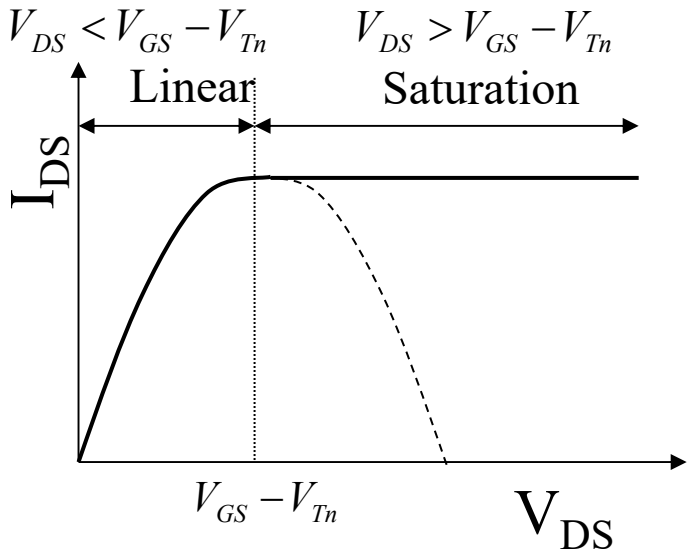
C_{OX} : GOX capacitance per area [F/m^2]

V_{Tn} : Threshold voltage @ V_{SB} = 0 [V]

Boundary between linear and saturation region

$$\frac{dI_{DS}}{dV_{DS}} = \beta_n \{(V_{GS} - V_{Tn}) - V_{DS}\} = 0$$

$$V_{DS} = V_{GS} - V_{Tn}$$



Model equation in saturation region

Gradual Channel Approximation + Boundary equation

$$V_{DS} = V_{GS} - V_{Tn}$$ // Boundary between linear and saturation region

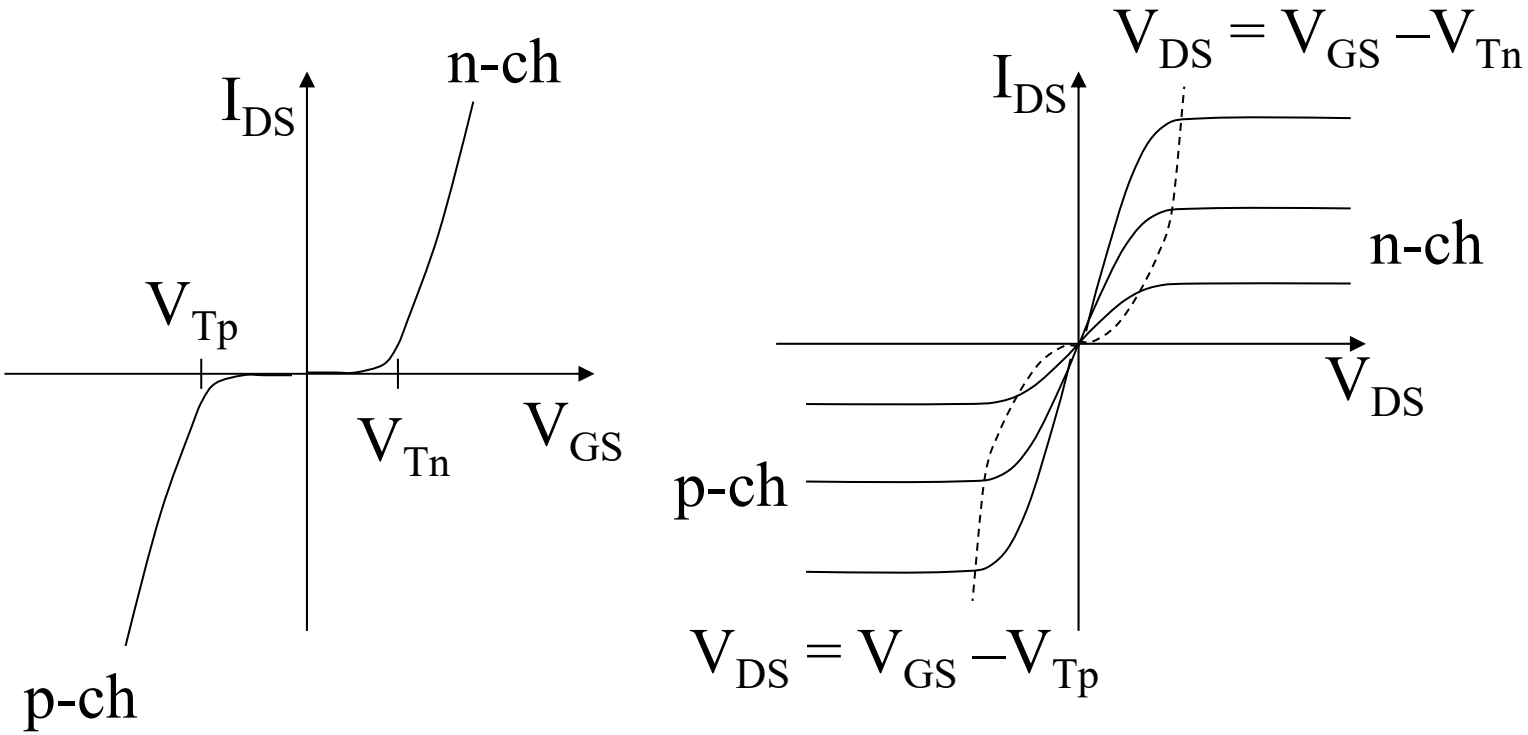
$$I_{DS} = \beta_n \{(V_{GS} - V_{Tn}) \cdot (V_{GS} - V_{Tn}) - \frac{1}{2}(V_{GS} - V_{Tn})^2\}$$

$$= \frac{\beta_n}{2}(V_{GS} - V_{Tn})^2$$

- 2nd order for V_{GS}
- No dependence on V_{DS}

p-ch and n-ch MOSFET

The n-ch MOSFET and p-ch MOSFET have a complementary characteristics.



I_{DS} : We assume direction flowing into a drain plus.

Gate overdrive voltage Δ_{OV}

Saturation condition: $V_{DS} > V_{GS} - V_T = \Delta_{OV}$

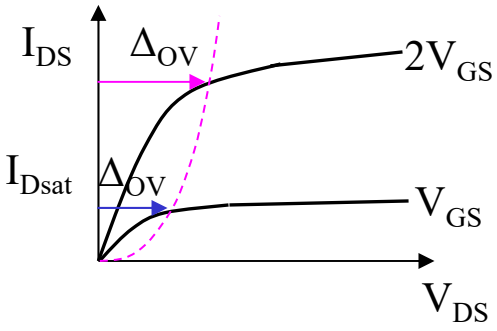
depends on I_{DS} and W/L.

$$\Delta_{OV} = V_{GS} - V_T = \sqrt{\frac{2I_{DS}}{\beta}} = \sqrt{\frac{2I_{DS}}{\mu \cdot C_{OX} \cdot (\frac{W}{L})}}$$

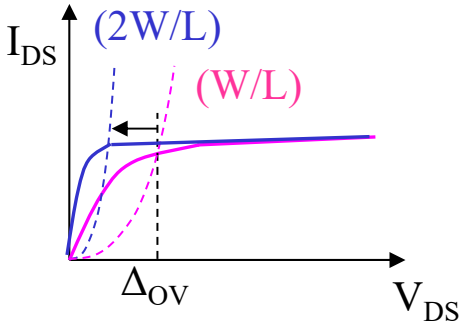
Bias Current

Bias voltage

(W/L) = const.



I_{DS} = const.

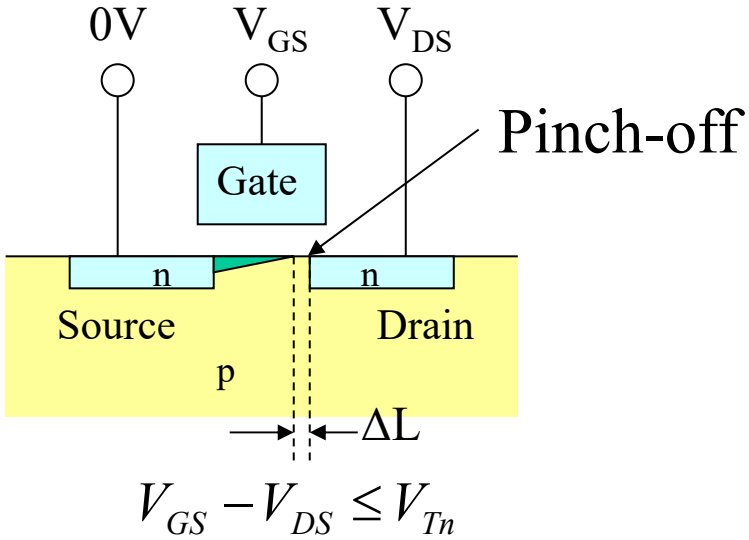


Chanel length modulation parameter

$V_{GS} - V_{DS} \le V_{Tn}$ (Saturating)

Channel length = $L_{eff} - \Delta L$

(ΔL is proportional to $V_{DS}^{0.5}$)

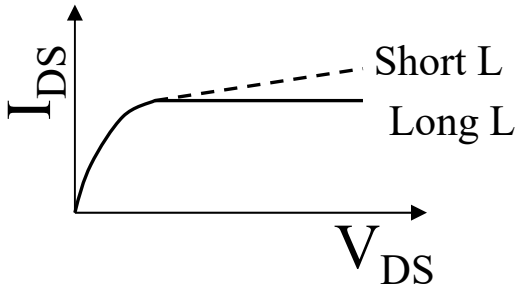


$V_{GS} - V_{DS} \le V_{Tn}$

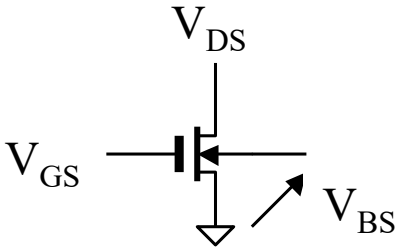
The drain current increases gradually after saturation, because the channel length is decreasing.

$$I_{DS} \cong \underbrace{\frac{\beta_n}{2}(V_{GS} - V_{Tn})^2}_{\text{Above-mentioned}} \{1 + \lambda \cdot (V_{DS} - \Delta_{OV})\}$$

Chanel length parameter (Lambda)



Substrate bias effect



$$V_{Tn} = V_{FB} + 2 \cdot \phi_B + \frac{1}{C_{OX}} \sqrt{2 \cdot \varepsilon_{Si} \varepsilon_0 \cdot q \cdot N_A (2 \cdot \phi_B - V_{BS})}$$

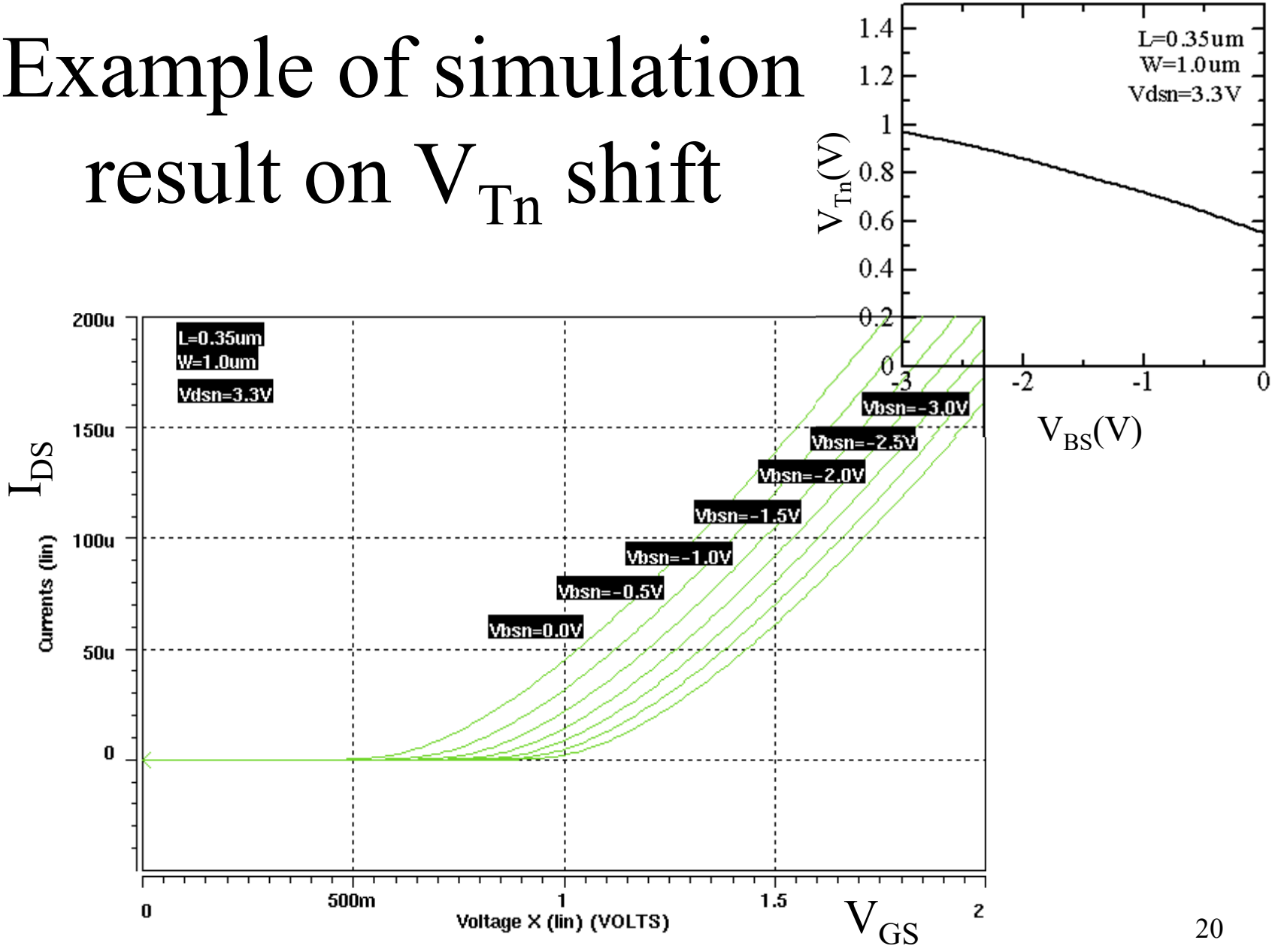
Impurity concentration in channel

Substrate bias

The V_{Tn} shifts upwards for $V_{BS} < 0$.

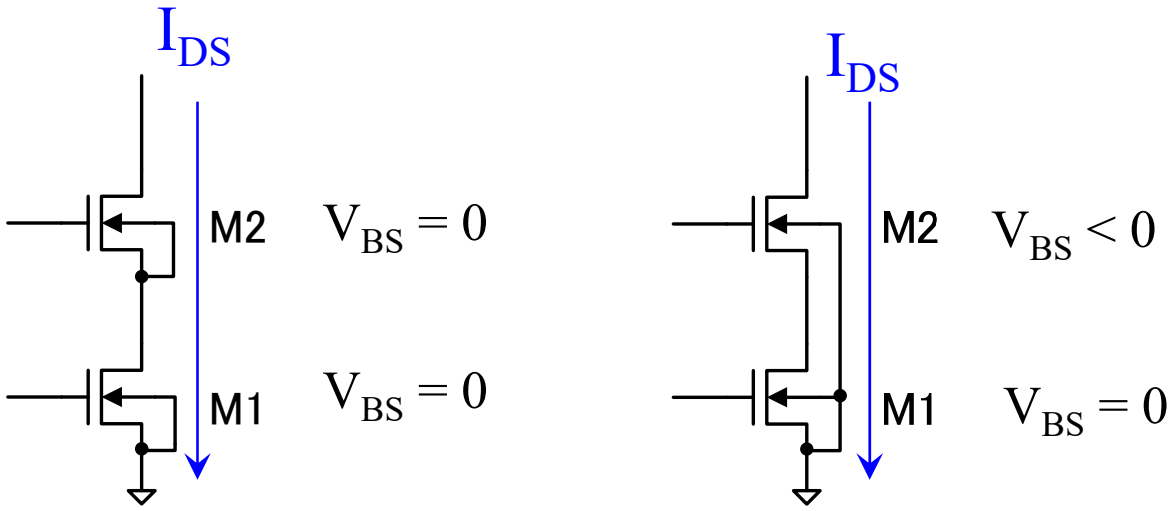
Some designer is applying this effect to control the threshold voltage of MOSFET, but the MOSFET cannot operate for $V_{BS} > 0$.

Example of simulation result on V_{Tn} shift



Substrate bias in the circuit operation

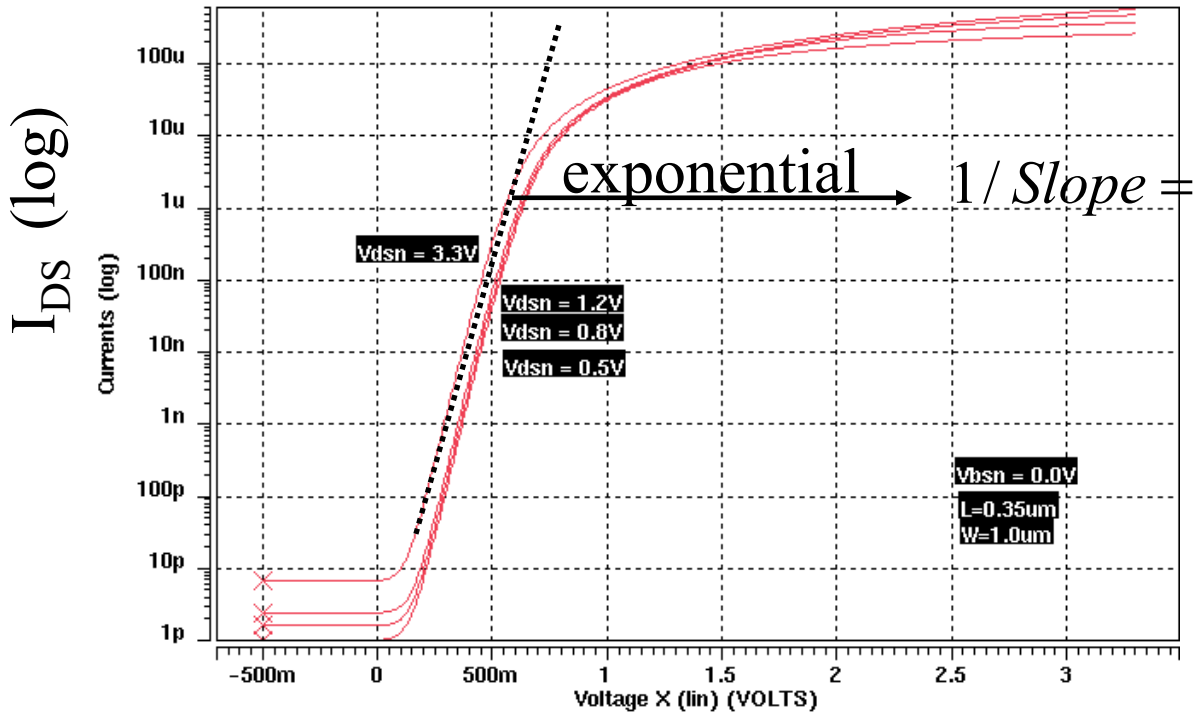
- The short-circuit with S and B of each transistor prevents substrate bias effect.
- However, the p-wells of M1 and M2 have to be electrically divided, because the well potential of M1 and M2 is different.



No substrate bias Normal connection

Sub-threshold Characteristic

Very small current I_{DS} is observed for $V_{GS} < V_{Tn}$



S factor

$$1/Slope = \frac{\partial V_{GS}}{\partial \log_{10}(I_{DS})} \equiv S$$

Model equation in sub-threshold region

$$V_{GS} < V_{Tn}$$

$$I_{DS} = \frac{W_n}{L_n} I_0 \exp\{\frac{q \cdot (V_{GS} - V_{Tn})}{m \cdot k_B T}\}$$

$$m = 1 + \frac{C_D}{C_{OX}}$$

Exponential for V_{GS}

I_{DS} depends on the channel width and temperature.
C_{OX}: GOX capacitance per area
C_D: Capacitance of MOS depletion layer per area

Model equations of n-ch MOSFET

V_{GS} \ V_{DS}	$V_{DS} < V_{GS} - V_{Tn}$	$V_{DS} > V_{GS} - V_{Tn}$
$V_{GS} > V_{Tn}$	$I_{DS} = \beta_n \{(V_{GS} - V_{Tn}) - \frac{1}{2} V_{DS}\} V_{DS}$ (Linear)	$I_{DS} = \frac{\beta_n}{2}(V_{GS} - V_{Tn})^2 \{1 + \lambda(V_{DS} - \Delta_{OV})\} \approx \frac{\beta_n}{2}(V_{GS} - V_{Tn})^2$ (Saturation)
$V_{GS} < V_{Tn}$ ($V_{DS} > 0.1V$)	$I_{DS} = \frac{W_n}{L_n} I_0 \exp\{\frac{q \cdot (V_{GS} - V_{Tn})}{m \cdot k_B T}\}$ (Sub-threshold)	

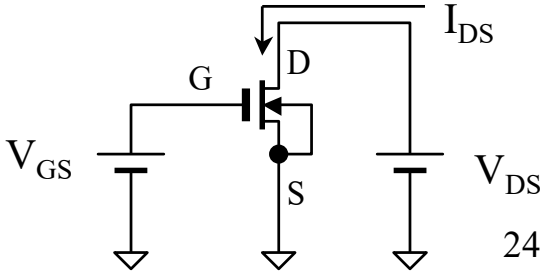
$$\beta_n = \frac{W_n}{L_n} \mu_n \cdot C_{OX} \qquad m = 1 + \frac{C_D}{C_{OX}}$$

$$C_{OX} = \varepsilon_0 \varepsilon_{SiO_2} \frac{1}{t_{OX}}$$

C_{OX}: GOX capacitance per area (F/m^2)

μ_n: Field effect mobility of electron ($m^2/Vsec$)

$V_{Tn} > 0$ (Enhancement mode)



Model equations of p-ch MOSFET

V_{GS} \ V_{DS}	$V_{DS} > V_{GS} - V_{Tp}$	$V_{DS} < V_{GS} - V_{Tp}$
$V_{GS} < V_{Tp}$	$I_{DS} = -\beta_p \{(V_{GS} - V_{Tp}) - \frac{1}{2} V_{DS}\} V_{DS}$ (Linear)	$I_{DS} = \frac{-\beta_p}{2}(V_{GS} - V_{Tp})^2 \{1 + \lambda(V_{DS} - \Delta_{OV})\} \approx \frac{\beta_p}{2}(V_{GS} - V_{Tp})^2$ (Saturation)
$V_{GS} > V_{Tp}$ ($V_{DS} < 0.1V$)	$I_{DS} = -\frac{W_p}{L_p} I_0 \exp\{\frac{q \cdot (V_{GS} - V_{Tp})}{m \cdot k_B T}\}$ (Sub-threshold)	

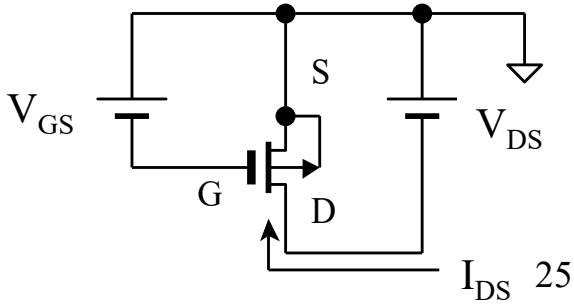
$$\beta_p = \frac{W_p}{L_p} \mu_p \cdot C_{OX} \qquad m = 1 + \frac{C_D}{C_{OX}}$$

$$C_{OX} = \varepsilon_0 \varepsilon_{SiO_2} \frac{1}{t_{OX}}$$

C_{OX}: GOX capacitance per area (F/m^2)

μ_n: Field effect mobility of hole ($m^2/Vsec$)

$V_{Tp} < 0$ (Enhancement mode)



7.3 DC characteristics of short channel MOSFET

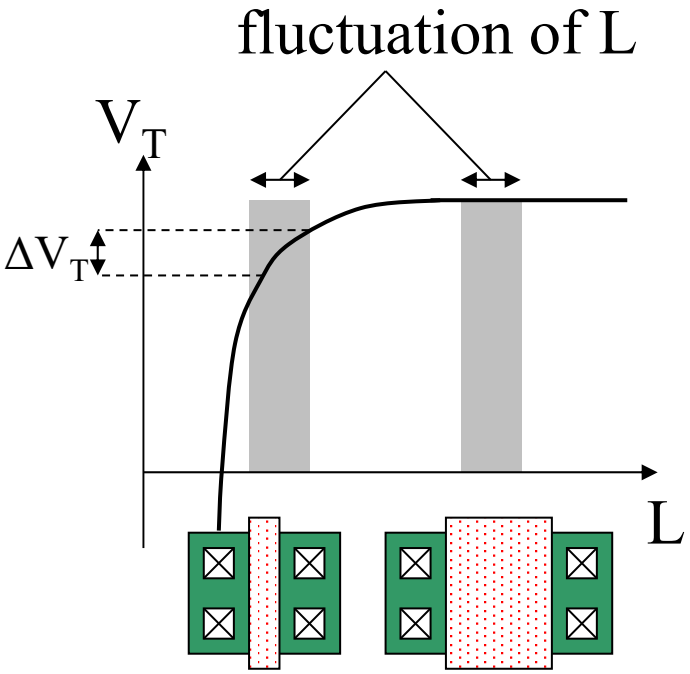
Influence of scaling down to L < 0.3μm

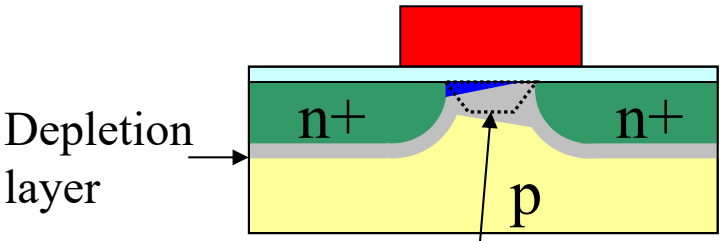
- Short channel effect
  - The threshold voltage V_T is decreased with decreasing L.
    - The three-dimensional distribution of the electric field in the MOSFET depends on an aspect ratio of cross section.
  - The I_{DS}-V_{GS} curve shows the linear characteristic in the saturation region and the boundary of linear and saturation region is obscured.
    - The strength of electric field in the channel is very high and the electron veracity in the channel is saturated.
  - The leak current of the sub-threshold region is increased.
    - The V_{DS} contributes the generation of the channel, and the tunneling current is increased with increasing the electric field of drain edge.

The simulation model considering to the short channel effect have to be used.

L-dependence of V_T

The fluctuation of V_T is sensitive to the fluctuation of L of the short channel MOSFET.

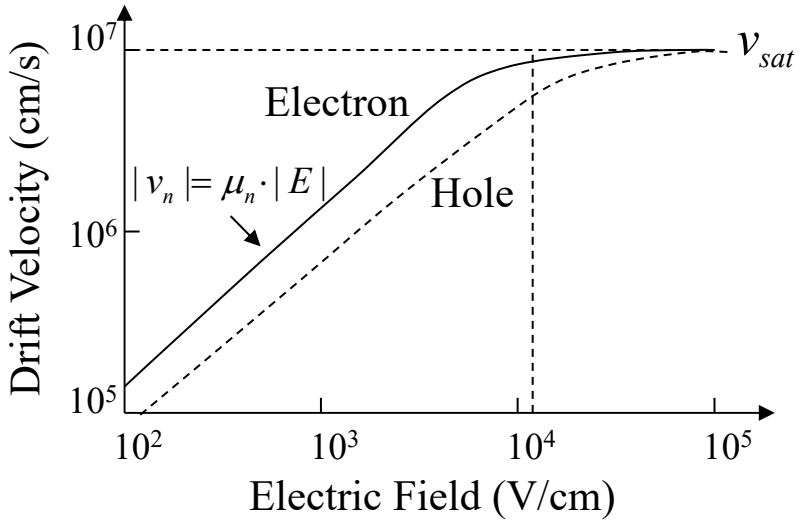




The amount of the charge controlled by V_{GS} is decreased with decreasing L. → The impurity concentration in channel is equivalently decreased and V_T is lowered.

Saturation of the drift velocity

Low electric field: Proportional to the strength of the electric field
High electric field: Saturated for the strength of the electric field



$$I_{DS} = \frac{\beta_n}{2}(V_{GS} - V_{Tn})^2$$

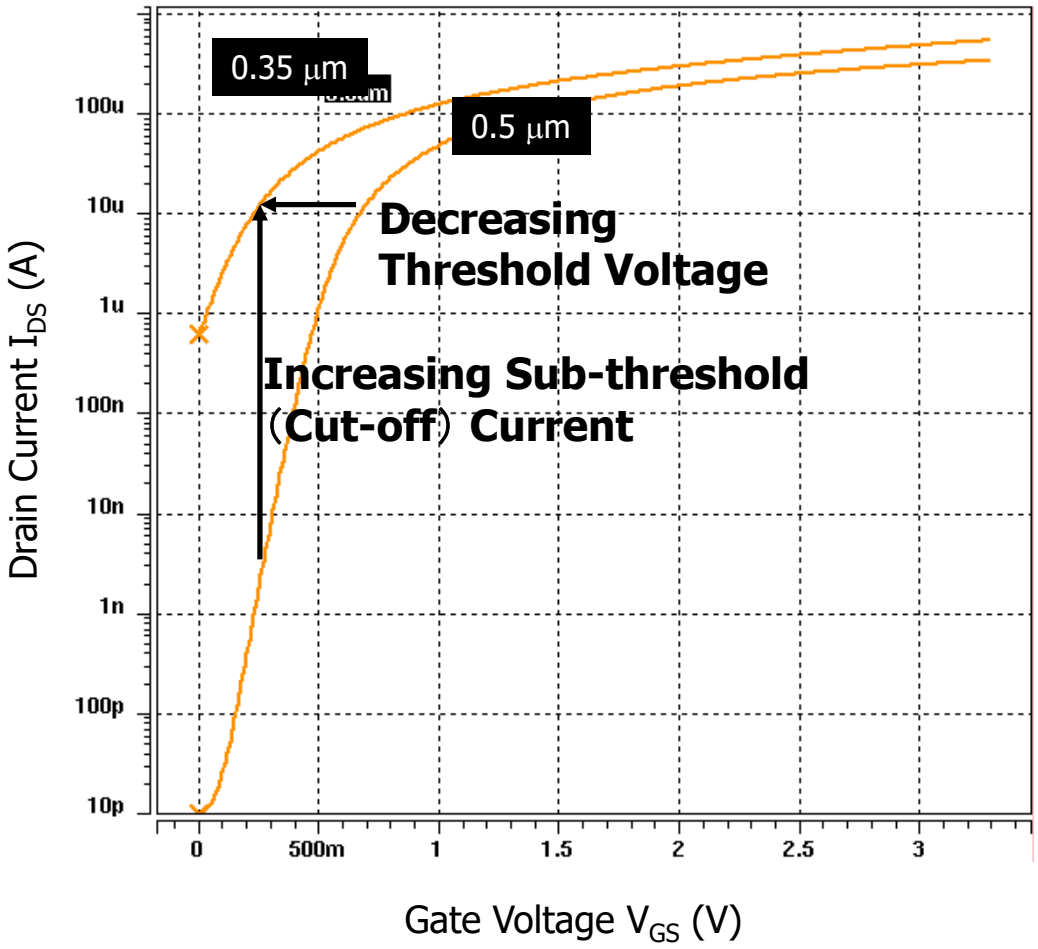
$$\beta_n = \frac{W_n}{L_n}\mu_n C_{OX}$$

$$\downarrow$$

$|v_n| = \mu_n \cdot |E|$ (low E)

$|v_n| = v_{sat}$ (high E)

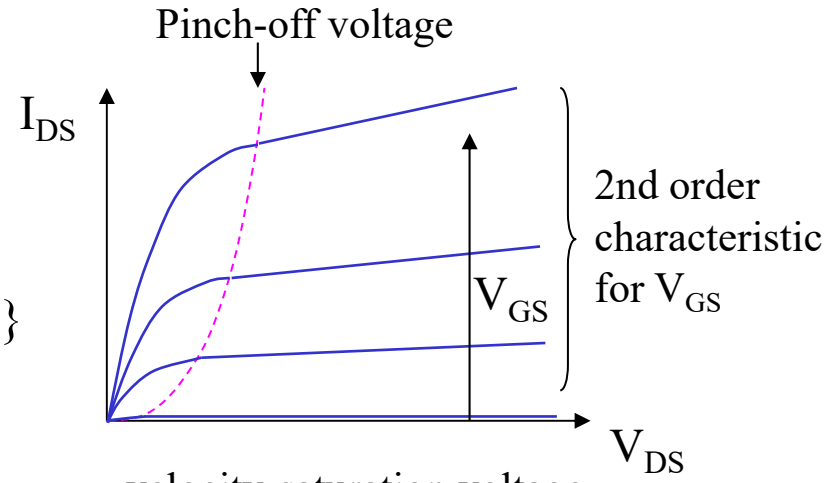
Degradation of S factor



Characteristics of Short channel MOSFET

Long Channel MOSFET

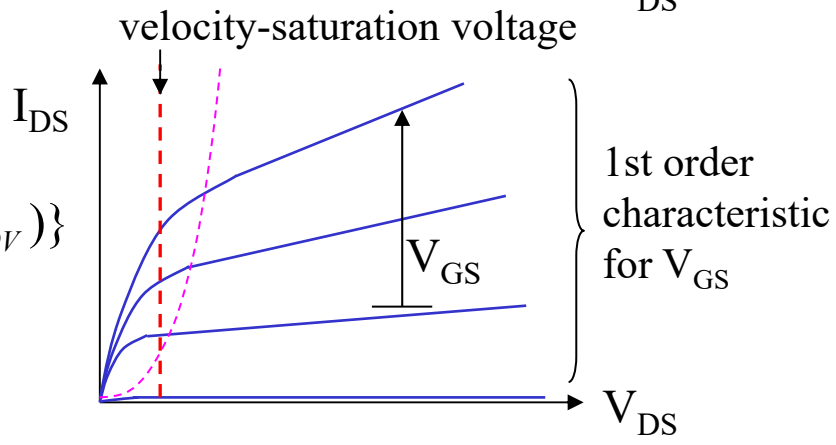
$$I_{DS} = \frac{\beta_n}{2}(V_{GS} - V_{Tn})^2\{1 + \lambda(V_{DS} - \Delta_{OV})\}$$



Short Channel MOSFET

$$I_{DS} = W_n \cdot v_{sat} \cdot C_{OX}(V_{GS} - V_{Tn})\{1 + \lambda(V_{DS} - \Delta_{OV})\}$$

v_{sat} : Saturation velocity of the carrier



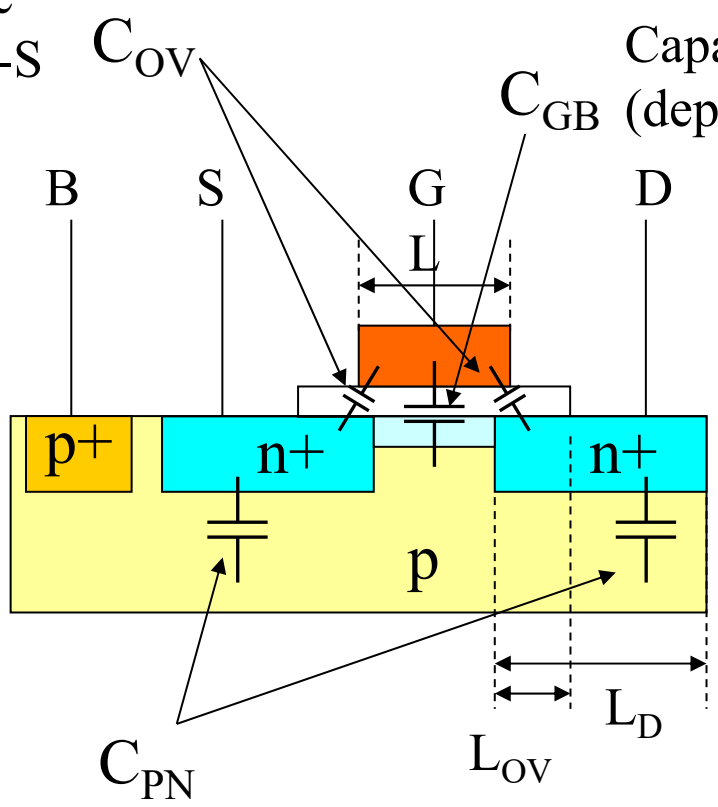
7.4 Capacitance-Voltage (C-V) characteristics

Parasitic capacitance in MOSFET

Overlap Capacitance between G-D and G-S (constant)

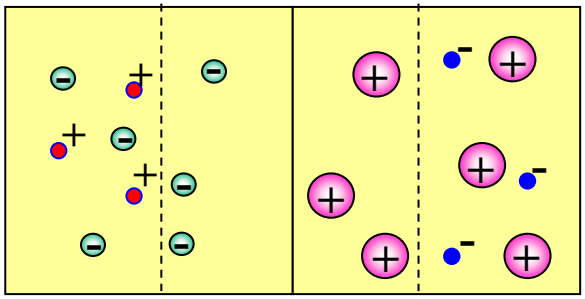
Capacitance between G-B (depending on the bias voltage)

Cross section



pn junction capacitance of D and S layer (depending on the bias voltage)

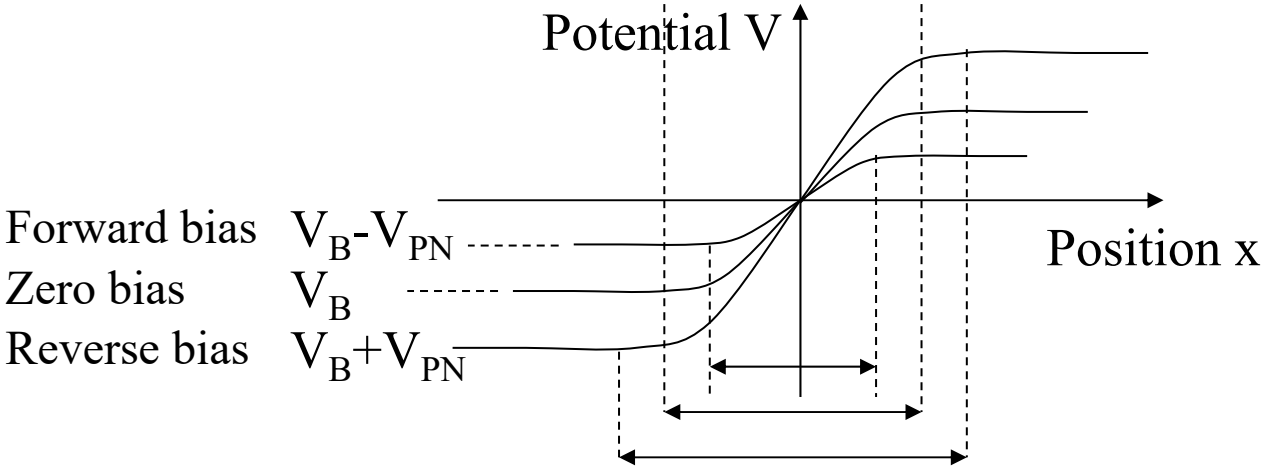
Bias dependence of pn junction capacitance (C_{PN}) -1



p-type n-type

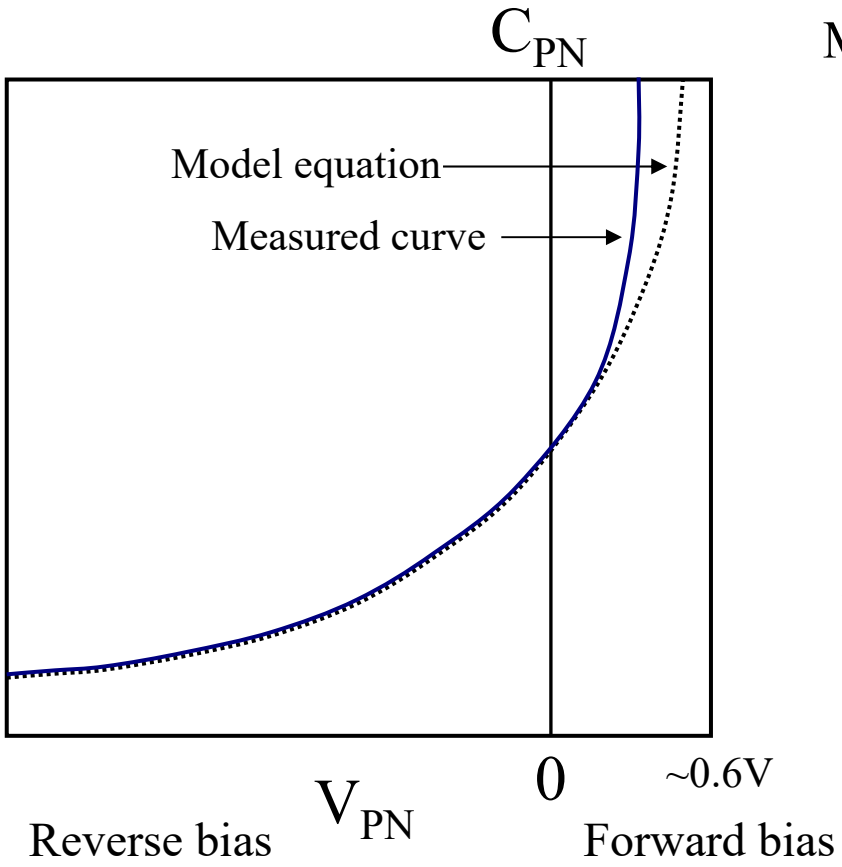
Depletion layer

The ionized donor and acceptor works as a electric double layer capacitor.



The width of depletion layer depends on the bias voltage.

Bias dependence of pn junction capacitance (C_{PN}) -2



Model equation of C-V characteristic

Junction area

$$C_{PN} = \varepsilon_0 \varepsilon_{Si} \frac{S}{d}$$ ← Depletion layer width

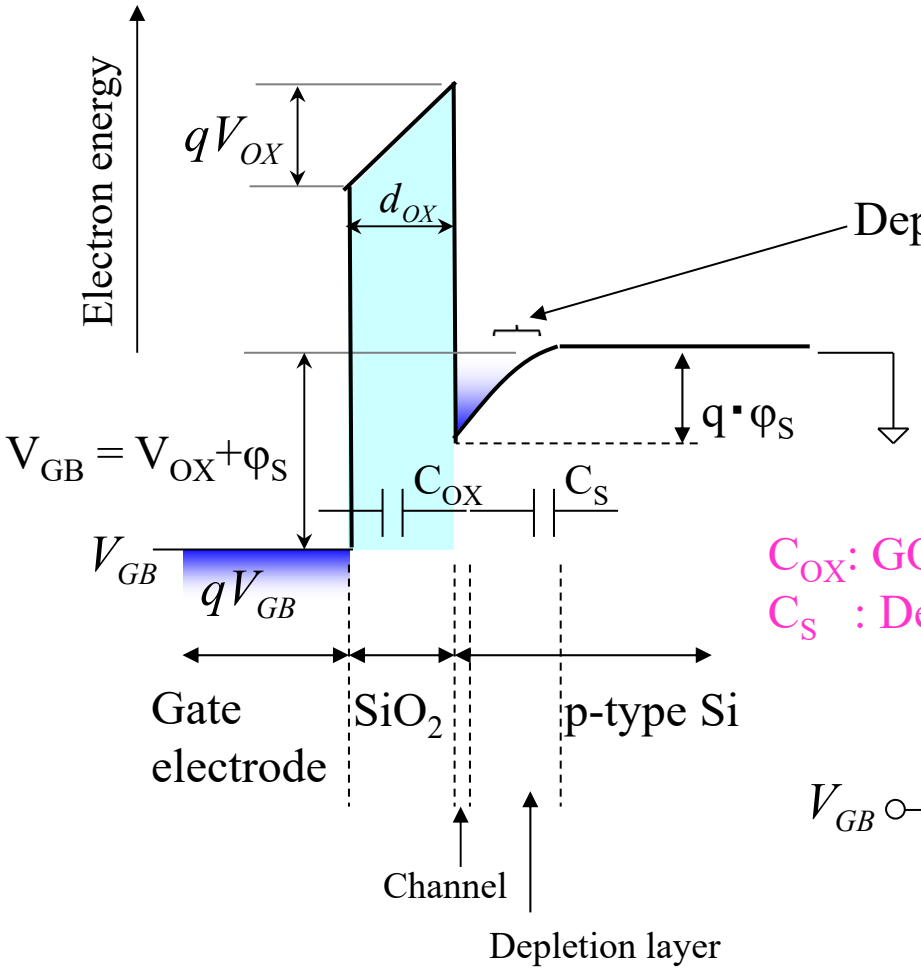
$$= \frac{C_{PN}(0V)}{\sqrt{1 - \frac{V_{PN}}{V_B}}}$$

V_B: Built-in Potential ~0.6～0.9V

NOTE: This equation is obtained according to depletion layer capacitance, and cannot be applicable to estimate the forward bias capacitance, because the injected minority carrier play a roll of a electric double layer capacitor (usually large value) in the high-level injection condition.

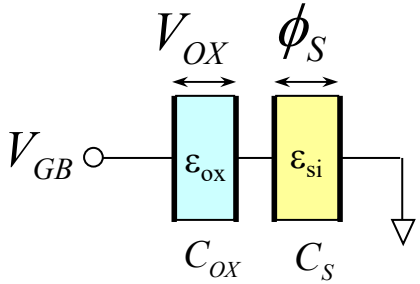
Bias dependence of MOS (C_{MOS}) -1

Electron energy lineup of the strong inversion for p-substrate MOS for $V_{GB} > V_{Tn}$



C_{OX}: GOX capacitance per area

C_S : Depletion layer capacitance per area



Equivalent circuit

$$V_{GB} = V_{OX} + \phi_S$$

$$\phi_S = \frac{C_{OX}}{C_{OX} + C_S} V_{GB}$$

Bias dependence of MOS (C_{MOS}) -2

In the weak inversion for p-substrate MOS for $V_{GB} < V_{Tn}$

Depletion layer and GOX capacitance per area

$$C_S = \frac{\varepsilon_0 \varepsilon_{Si}}{x_D}$$

$$C_{OX} = \frac{\varepsilon_0 \varepsilon_{SiO_2}}{t_{OX}}$$

Width of depletion layer

$$x_D = \sqrt{\frac{2\varepsilon_0 \varepsilon_{Si} \phi_S}{qN_A}}$$

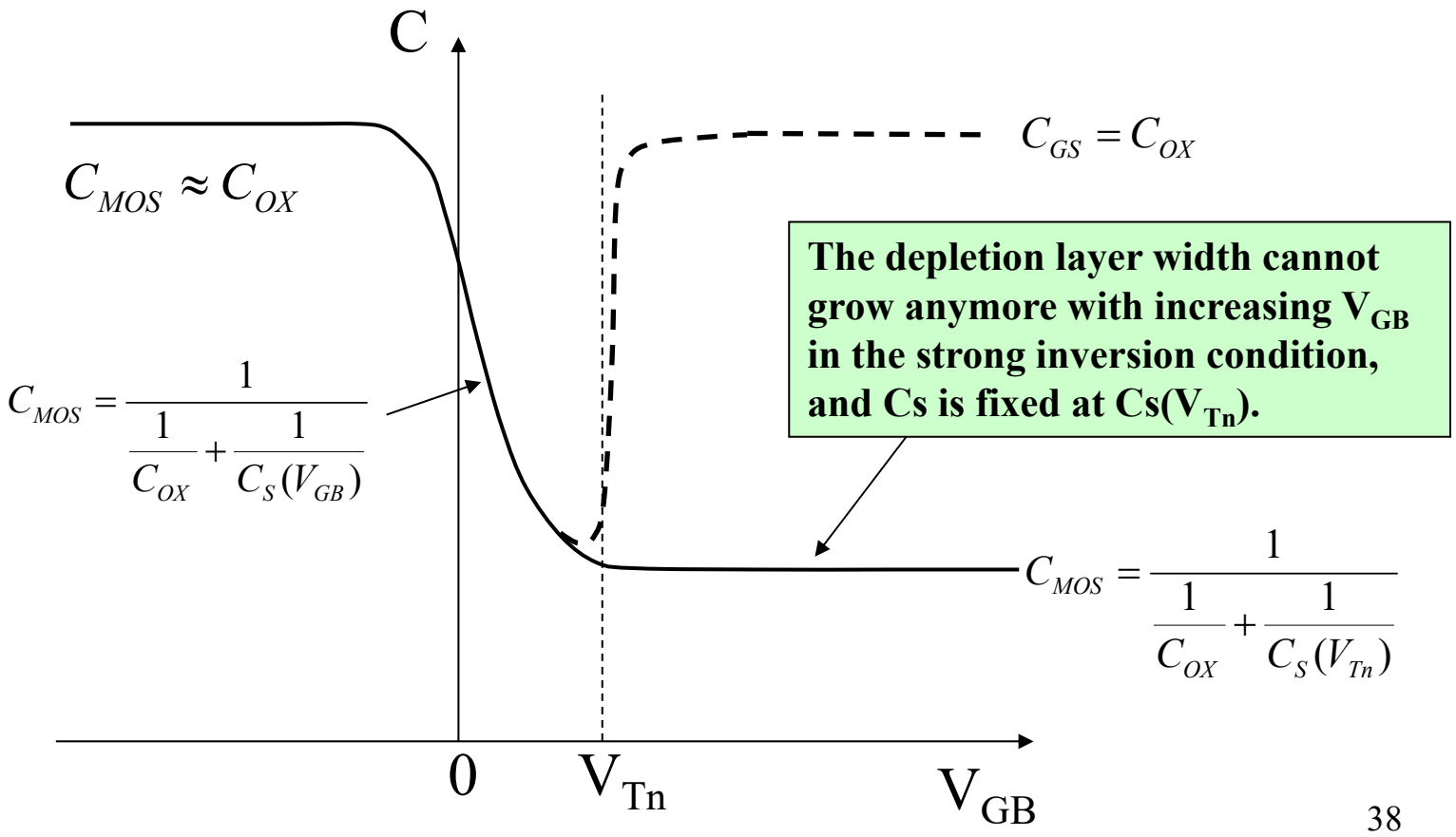
$$\phi_S = \frac{C_{OX}}{C_{OX} + C_S} V_{GB}$$

Total capacitance

$$C_{MOS} = \frac{1}{\frac{1}{C_{OX}} + \frac{1}{C_S}}$$

Bias dependence of MOS (C_{MOS}) -3

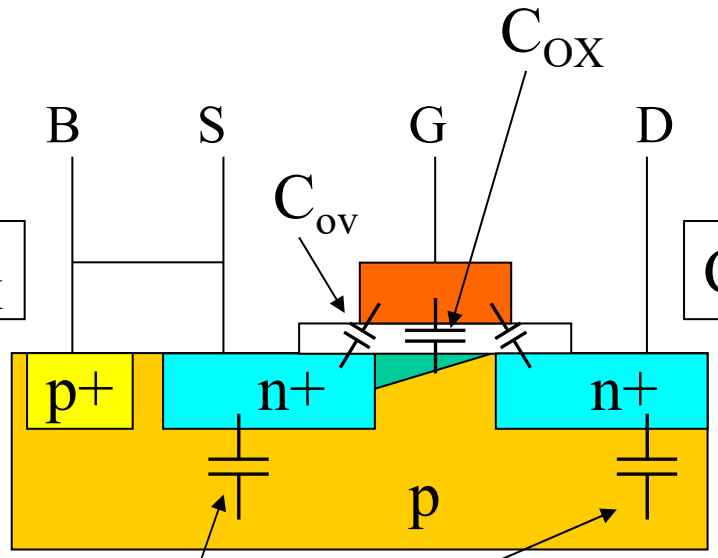
C-V characteristic of MOS capacitor



Interelectrode capacitance of MOSFET

$C_{gs} = C_{ov} + \alpha(V) \cdot C_{OX}$

The variable α(V) depends on the bias condition.
α(V) ~ 2/3 in the strong inversion condition (linear region and saturation region).

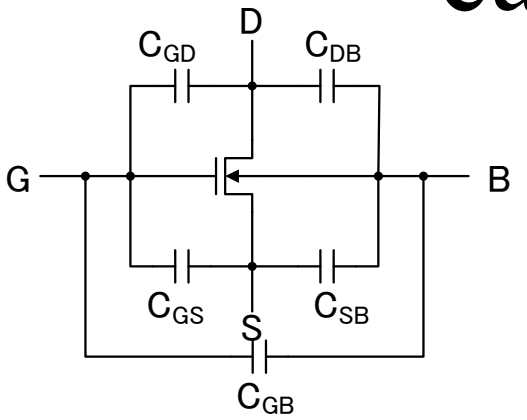


$C_{gd} = C_{ov}$

$C_{ds} = C_j$

$$C_j(V) = \frac{C_j(0)}{\sqrt[2\sim3]{1 + \frac{V}{2\phi_B}}}$$

Model of interelectrode capacitance



Capacitance independent on bias
- CGDO: G-D overlap capacitance
- CGSO: G-S overlap capacitance
- CGBO: G-B overlap capacitance

Label	Sub-threshold region	Linear region	Saturation region
C_{GD}	CGDO*W	$0.5*C_{OX}*W*L$	CGDO*W
C_{DB}	C_j*W*L_D	C_j*W*L_D	C_j*W*L_D
C_{GB}	$C_{OX}*W*L_{eff}$	CGBO*L	CGBO*L
C_{GS}	CGSO*W	$0.5*C_{OX}*W*L$	$2/3*C_{OX}*W*L$
C_{SB}	C_j*W*L_S	C_j*W*L_S	C_j*W*L_S

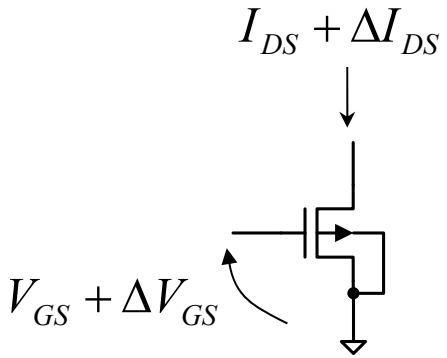
7.5 Small-signal characteristics

Biasing for MOSFET operation

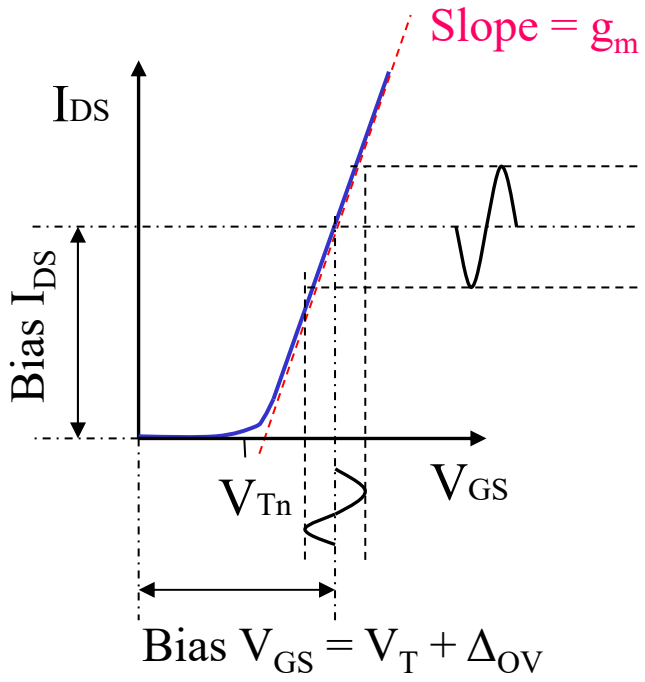
- Analog circuit operates with DC biasing
  - The MOSFETs are operated in the saturation region and sometimes in the linear region and sub-threshold region if needed.
  - The small-signal parameters depends on the bias current I_{DS} in the saturation region.
  - The bias current I_{DS} is designed with the circuit parameter V_{GS} and W/L.
- Digital circuit does not require the concept of biasing
  - Logic value '1' ← Linear(p-ch), Sub-threshold(n-ch)
  - Logic value '0' ← Linear(n-ch), Sub-threshold(p-ch)
  - '1' ⇔ '0' transition = Saturation region(p-ch and n-ch)

Transconductance g_m (1)

The transconductance g_m expresses ability for amplification of the MOSFET.



$$y_{21} = g_m = \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{V_{DS}}$$



NOTE: Small-signal parameters of p-ch and n-ch MOSFET are given by the same expression, because the small-signal parameters connected to the slope of the DC characteristics.

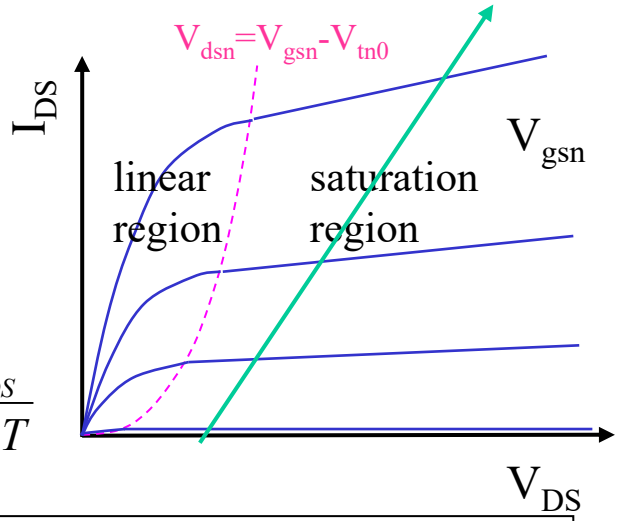
Transconductance g_m (2)

Bias current dependence of g_m

$V_{GS} < V_{Tn}$ (Sub-threshold region)

$$I_{DS} = \frac{W_n}{L_n} I_0 \exp\{\frac{q \cdot (V_{GS} - V_{Tn})}{m \cdot k_B T}\}$$

$$g_m = \frac{W_n}{L_n} I_0 \frac{q}{m \cdot k_B T} \exp\{\frac{q \cdot (V_{GS} - V_{Tn})}{m \cdot k_B T}\} = \frac{q \cdot I_{DS}}{m \cdot k_B T}$$



$V_{GS} > V_{Tn}$ (Saturation region)

Long Channel ($E_{sat} \cdot L >> V_{GS}-V_{Tn}$)

$$I_{DS} = \frac{\beta_n}{2}(V_{GS} - V_{Tn})^2$$

$$g_m = \beta_n (V_{GS} - V_{Tn}) = \sqrt{2\beta_n \cdot I_{DS}}$$
$$= \frac{2I_{DS}}{V_{GS} - V_{Tn}}$$

Velocity saturation MOSFET

Short Channel ($E_{sat} \cdot L < V_{GS}-V_{Tn}$)

$$I_{DS} = v_{sat} W C_{OX} (V_{GS} - V_{Tn})$$

$$g_m = v_{sat} W C_{OX}$$

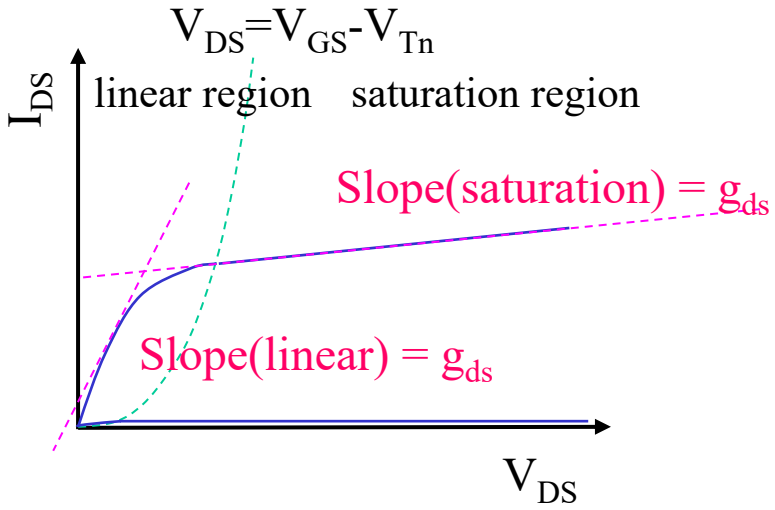
Output conductance g_{ds}

g_{ds} in saturation region

$$I_{DS} = \frac{\beta_n}{2}(V_{GS} - V_{Tn})^2\{1 + \lambda(V_{DS} - \Delta_{OV})\}$$

$$y_{22} = g_{ds} = \frac{\partial I_{DS}}{\partial V_{DS}} = \frac{\beta_n}{2}(V_{GS} - V_{Tn})^2 \cdot \lambda$$

$$\cong \lambda \cdot I_{DS} \qquad (V_{DS} > V_{GS} - V_{Tn})$$

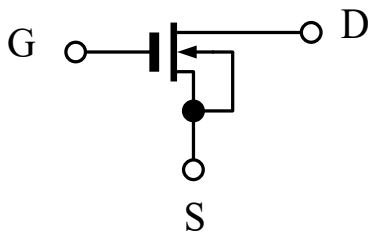


g_{ds} in linear region

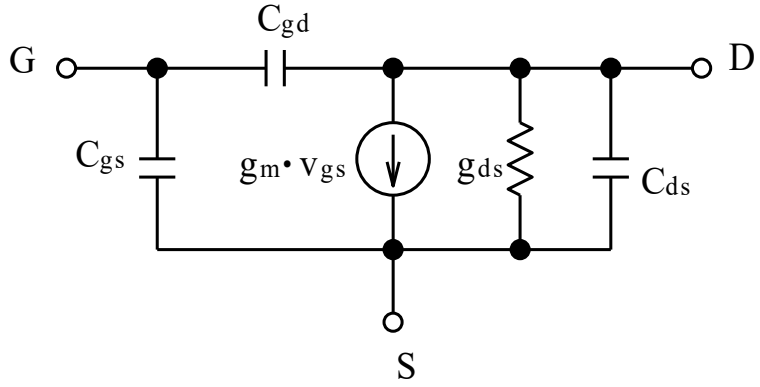
$$I_{DS} = \beta_n\{(V_{GS} - V_{Tn}) \cdot V_{DS} - \frac{1}{2}V_{DS}^2\}$$

$$y_{22} = g_{ds} = \frac{\partial I_{DS}}{\partial V_{DS}} = \beta_n\{(V_{GS} - V_{Tn}) - V_{DS}\} \qquad (V_{DS} < V_{GS} - V_{Tn})$$

y parameters of MOSFET



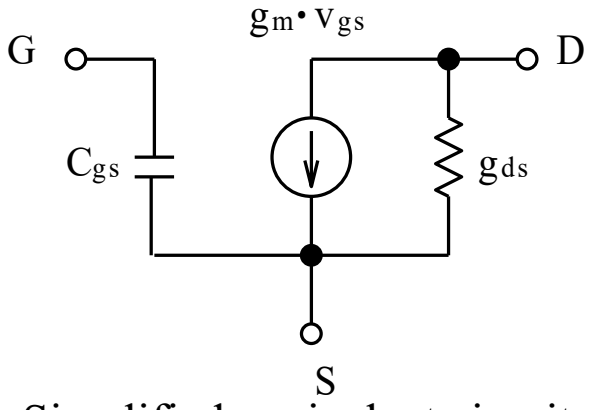
Small-signal equivalent circuit



Small-signal equivalent circuit (C_{gs} includes C_{gb})

$$\begin{bmatrix} i_{gs} \\ i_{ds} \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} v_{gs} \\ v_{ds} \end{bmatrix}$$

$$\begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} = \begin{bmatrix} j\omega \cdot C_{gs} & 0 \\ g_m & g_{ds} \end{bmatrix}$$

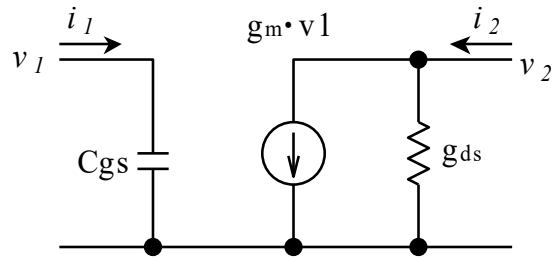


$$g_m = \sqrt{2\beta_n \cdot I_{DS}}$$

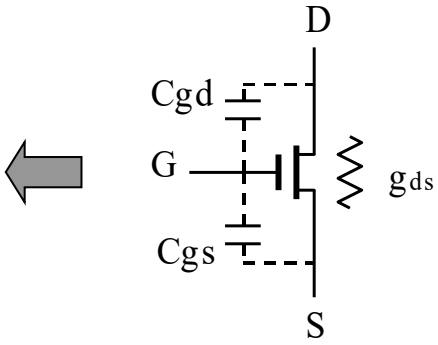
$$g_{ds} = \lambda_n \cdot I_{DS}$$

Simplified equivalent circuit
(C_{gs} >> C_{gd} in a saturation region)

h parameters of MOSFET



Small-signal equivalent circuit



$$\begin{bmatrix} v_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} i_1 \\ v_2 \end{bmatrix}$$

$$\begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} = \begin{bmatrix} \dfrac{1}{j\omega \cdot C_{gs}} & 0 \\ \dfrac{g_m}{j\omega \cdot C_{gs}} & g_{ds} \end{bmatrix}$$

Transition Frequency

$$when \quad f = f_T, \ |h_{21}| = 1 \quad (= 0\text{dB})$$

$$f_T = \frac{g_m}{2\pi \cdot C_{gs}}$$

where g_m depends on W/L and I_{DS} (long channel)

$$h_{21} = \left. \frac{i_2}{i_1} \right|_{v_2 = 0} = \frac{g_m}{j\omega \cdot C_{gs}} \quad \longleftarrow \quad \begin{cases} i_1 = j\omega \cdot C_{gs} \cdot v_1 \\ i_2 = g_m \cdot v_1 \qquad (v_2 = 0) \end{cases}$$

Transition Frequency f_T

The frequency for the current gain $h_{21} = 1$

Long channel MOS

$$I_{DS} = \frac{\beta}{2}(V_{GS} - V_T)^2$$

$$\beta = \mu \cdot C_{OX} \cdot \frac{W}{L}$$

$$g_m = \frac{dI_{DS}}{dV_{GS}} = \sqrt{2\beta \cdot I_{DS}}$$

$$f_T = \frac{\sqrt{2\beta \cdot I_{DS}}}{2\pi \cdot C_{gs}}$$

depending on the bias current

Short channel MOS

$$I_{DS} = v_{SAT} C_{OX} W (V_{GS} - V_T)$$

$$g_m = \frac{dI_{DS}}{dV_{GS}} = v_{SAT} C_{OX} W$$

$$f_{T\_peak} = \frac{v_{SAT} C_{OX} W}{2\pi \cdot C_{gs}} = \frac{v_{SAT} C_{OX} W}{2\pi \cdot C_{OX} WL} = \frac{v_{SAT}}{2\pi \cdot L}$$

independent on the bias

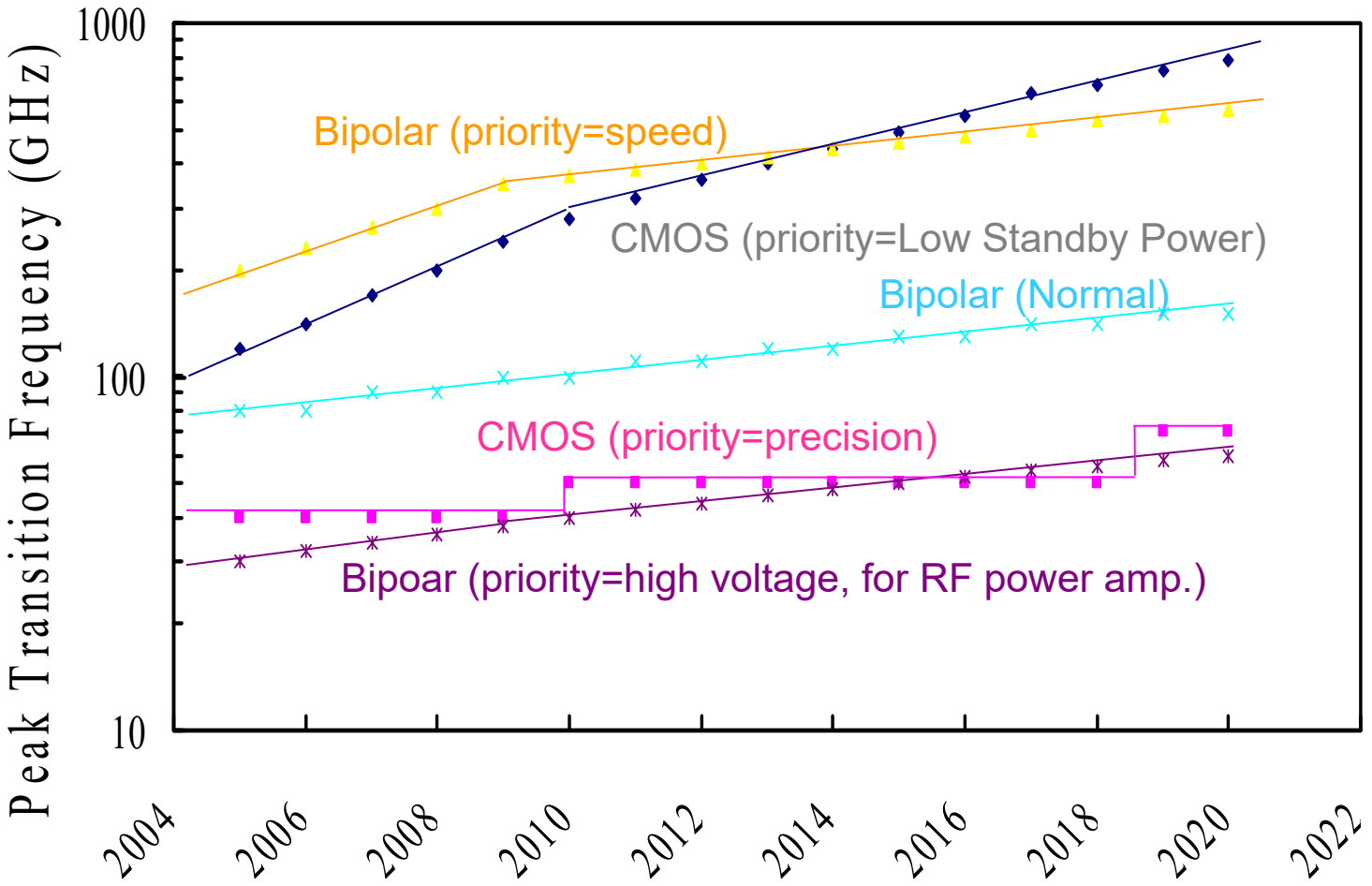
[Ref.] g_m of bipolar junction transistor (BJT)

$$I_B = I_S(e^{\frac{qV_{BE}}{kT}} - 1)$$

$$\frac{dI_B}{dV_{BE}} \cong \frac{q}{kT} I_B$$

$$g_m = \frac{dI_C}{dV_{BE}} = \frac{dI_B}{dV_{BE}} \frac{dI_C}{dI_B} \cong \frac{q}{kT} I_B \cdot h_{fe} = \frac{q}{kT} I_C$$

RF and mixed signal technology trend



Circuit performance depending on Δ_{OV}

Voltage gain

$$I_{DS} = \frac{\beta_n}{2}(V_{GS} - V_{Tn})^2 = \frac{\beta_n}{2}\Delta_{OV}^2$$

$$\Delta_{OV} = \sqrt{\frac{2I_{DS}}{\beta_n}}$$

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \beta_n \Delta_{OV}$$

$$|Gain| = \frac{g_m}{g_{ds}} \propto \frac{g_m}{I_{DS}} = \frac{2}{\Delta_{OV}}$$

Small Δ_{OV} is better.

Tolerance for V_T fluctuation

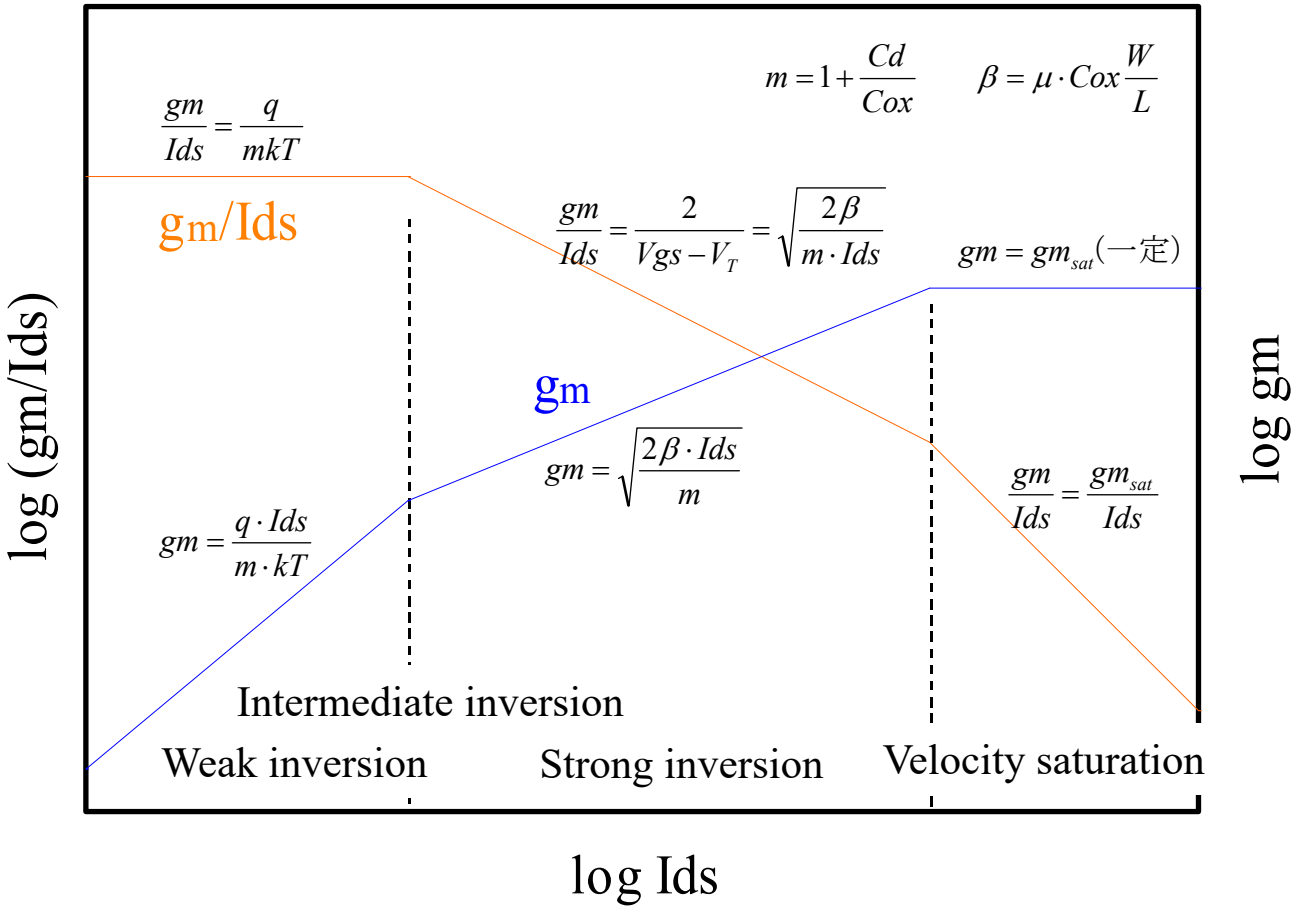
$$\frac{\partial I_{DS}}{\partial V_{Tn}} = -\beta_n \Delta_{OV}$$

$$\frac{\partial I_{DS}}{I_{DS}} = -\beta_n \Delta_{OV} \frac{\partial V_{Tn}}{I_{DS}} = -2\frac{\partial V_{Tn}}{\Delta_{OV}}$$

Large Δ_{OV} is better.

Bias current dependence of g_m

The previous equations are simplified assuming m =1. The parameter m is derived from the dependence of C_d on V_{GS}.



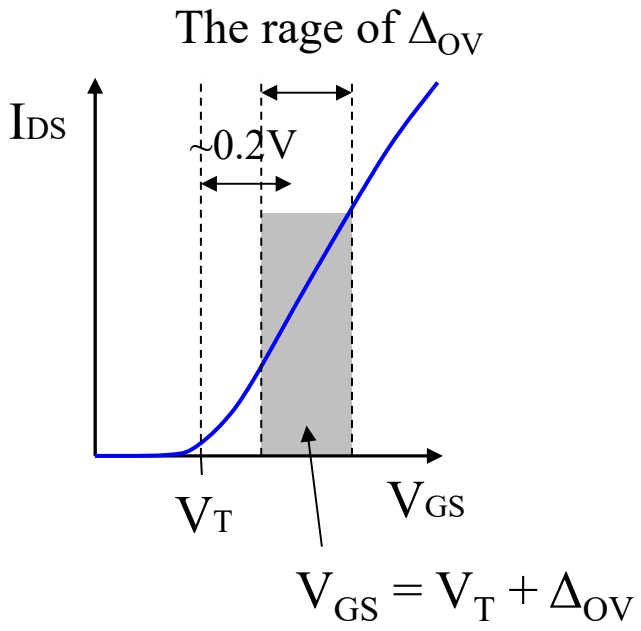
[Important] Optimization of Δ_{OV}

- Δ_{OV} depends on W/L, and I_{DS}.
- g_m and the production tolerance depends on Δ_{OV}. Therefore, there is a reasonable range in a value of Δ_{OV}.
- The value of V_{GS} is usually chosen among the range of

Δ_{OV} = 0.15V~0.30V

Typically Δ_{OV} = 0.2V

(See the slide 64.)



7.6 Inherent noise

Quantification of the noise

PSD: Power Spectrum Density of noise

$$PSD = \overline{v_{noise}^2(f)} \qquad (V^2/Hz)$$

RMS noise voltage in the band from f_L to f_H

$$\sqrt{\int_{f_L}^{f_H} \overline{v_{noise}^2(f)} \cdot df} \qquad (V)$$

RMS noise power in the band from f_L to f_H

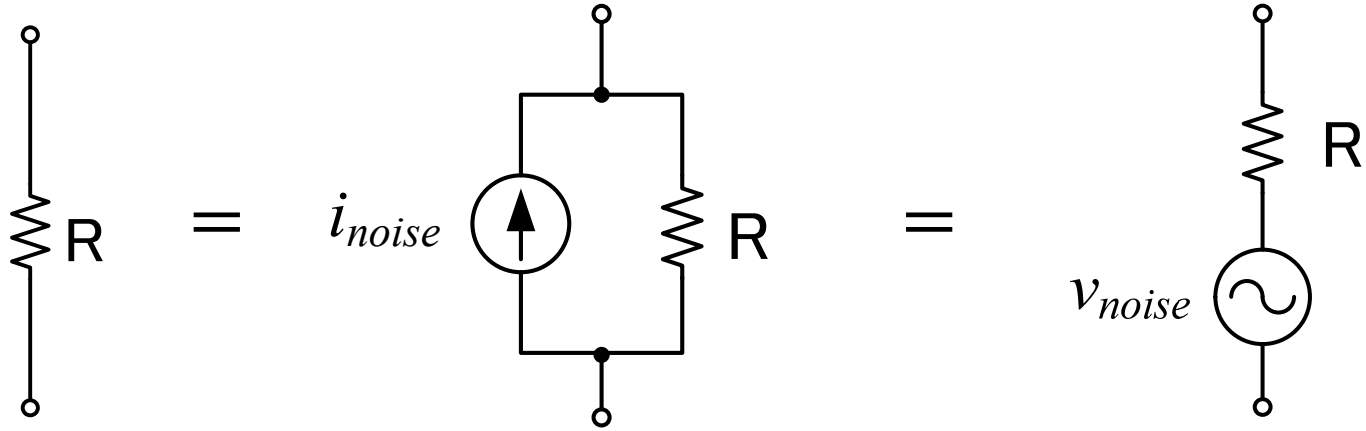
$$\frac{1}{R}\int_{f_L}^{f_H} \overline{v_{noise}^2(f)} \cdot df \qquad (W)$$

Source of inherent noise

1. Thermal noise (Johnson noise)
   - Random movement of carrier in all conductive material
   - White noise
   - independent on the bias
2. Flicker noise
   - Random ionization of deep level trap in semiconductors
   - 1/f noise（$1/f^n$, where n=0.8～1.3）
   - dependent on the bias
   - inversely proportional to L*W of MOSFET
3. Shot noise (modeled after BSIM4)
   - Statistical fluctuation of thermal emission and tunneling through the potential barrier in semiconductors
   - White noise
   - proportional to voltage
   - observed in the short channel MOSFET (t_{ox} < 20nm)

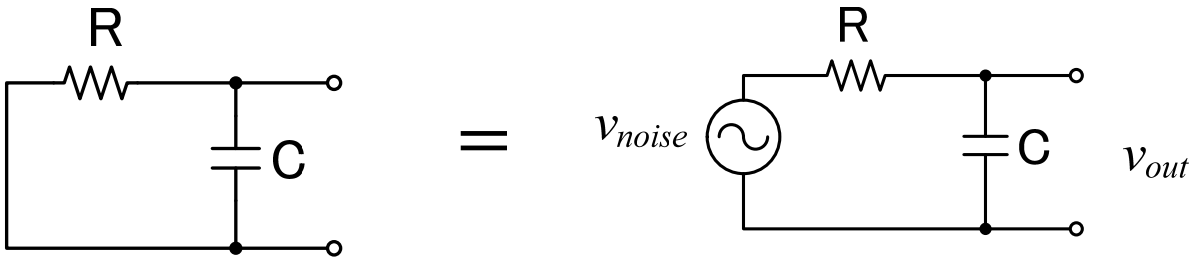
The noise model is implemented in the device model of the circuit simulators, but a measured parameter may not be provided by semiconductor manufacture.

Thermal noise of resistor



$$\overline{i_{noise}^2} = \frac{4kT}{R} \text{ (A}^2\text{/Hz)} \qquad \overline{v_{noise}^2} = 4kTR \text{ (V}^2\text{/Hz)}$$

Thermal noise of RC circuit



$$v_{out} = \frac{1}{1 + j\omega CR} v_{noise} = \frac{1}{1 + j\omega/\omega_p} \quad , \qquad \omega_p = \frac{1}{CR}$$

$$\overline{v_{out}^2} = \frac{\overline{v_{noise}^2}}{1 + \omega^2/\omega_p^2}$$

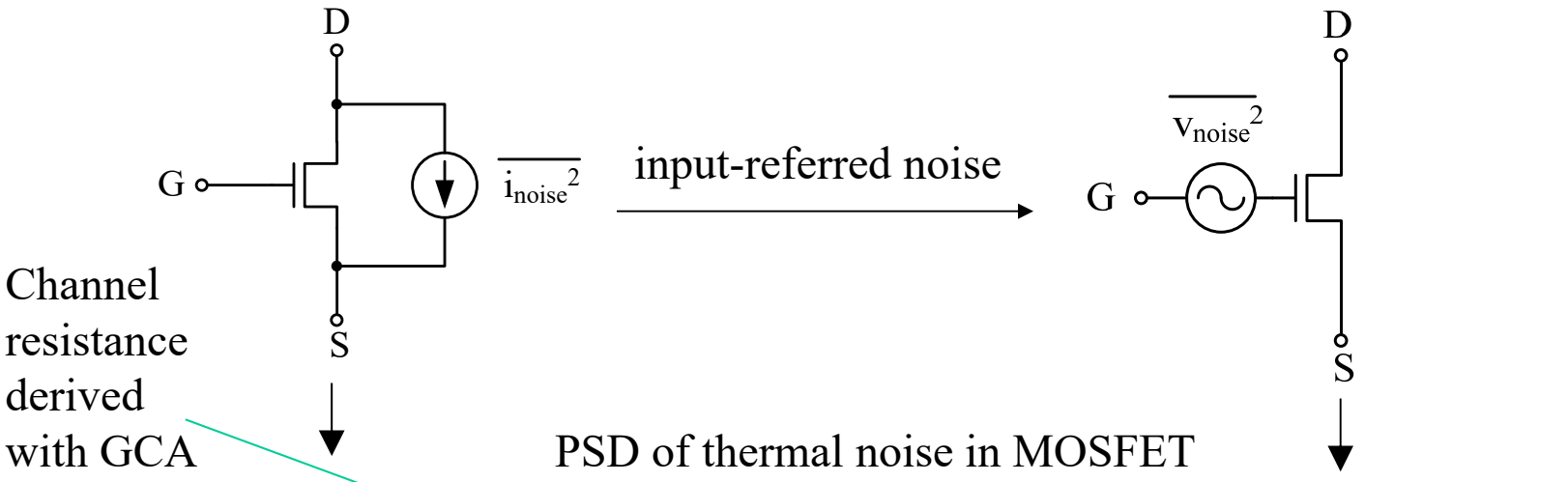
$$RMS(\overline{v_{out}}) = \sqrt{\int_0^\infty \overline{v_{out}^2}\, d\omega} = \sqrt{\frac{kT}{C}}$$

Large C suppresses the thermal noise generated by the resistor, but the time constant of the circuit is increased.

NOTE: The RMS of thermal noise v_{out} is limited by the size of the capacitor, and independent of the size of the resistor. The thermal noise can be observed in you remove the resistor, because the charge stored in the capacitor is fluctuating.

Thermal noise of MOSFET

PSD of the thermal noise depends on the conductance.



$$\overline{i_{noise}^2} = 4 \cdot k_B T \cdot \gamma \cdot \frac{2}{3} g_m \quad \text{(Saturation region)}$$

$$\overline{v_{noise}^2} = \frac{\overline{i_{noise}^2}}{g_m^2} = \frac{8 k_B T \cdot \gamma}{3 g_m}$$

$\gamma = 1$ (Long Channel > 0.25μm)

2 (Short Channel < 0.25μm)

Normally this equation is used.

Limitation of the gate width

PSD of the gate resistance noise

$$\overline{v_{noise}^2} = 4k_B T \cdot R_G = 4k_B T \cdot R_{\square} \frac{W}{L}$$

PSD of the channel resistance noise

$$\overline{v_{noise}^2} = \frac{8k_B T \cdot \gamma}{3g_m}$$

W/L is limited according to the thermal noise condition:
Gate resistance noise < Channel resistance

$$R_{\square} \frac{W}{L} \leq \frac{2}{3} \frac{\gamma}{g_m} \approx \frac{1}{g_m}$$

Flicker noise of MOSFET

PSD of the Flicker noise depends on the L*W.

$$\overline{v_{noise}^2} = \frac{K_F}{C_{OX}^{\ 2} \cdot W \cdot L} \frac{1}{f^n}$$

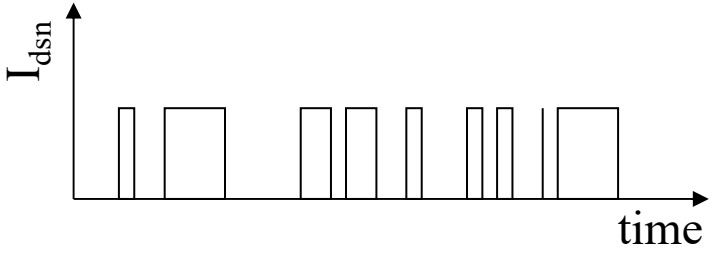
Designed

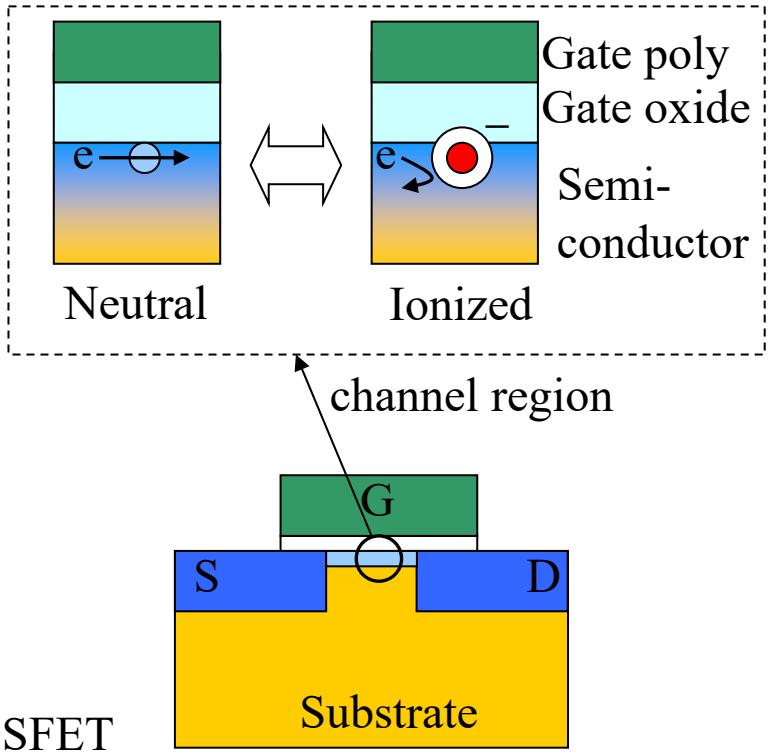
$K_F \approx 10^{-24}$ (V^2F) (n-ch)

$\approx 10^{-25}$ (V^2F) (p-ch)

$n \approx 0.8 \sim 1.3$

Flicker noise coefficient depending on the process



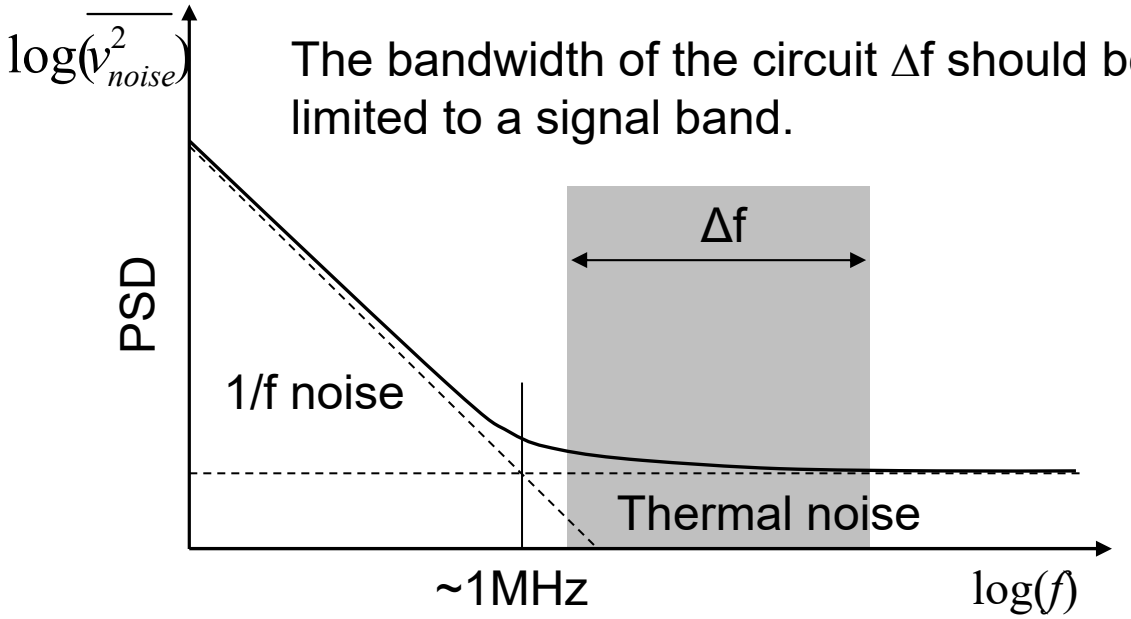


Quantized Flicker noise of Ultra-narrow-W MOSFET

PSD of dominant noise in MOSFET

- The 1/f noise is an intrinsic noise in semiconductors.
- The thermal noise occurs anywhere in conductor.

Effective noise voltage = $\sqrt{\overline{v_{noise}^2} \cdot \Delta f}$



SNR and NF

Noise strength mixed in the signal

SNR: Signal to Noise Ratio

Noise voltage

$$SNR(dB) = 20\log_{10}\frac{|V_{signal}|}{|V_{noise}|}$$

Noise power

$$SNR(dB) = 10\log_{10}\frac{|P_{signal}|}{|P_{noise}|}$$

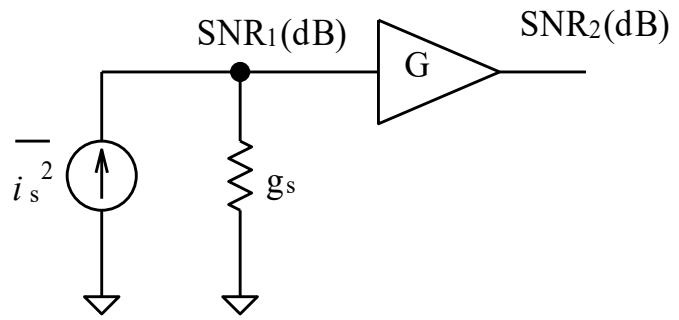
NOTE: The absolute noise strength is often given by the input-referred noise power (dBm).

Noise strength generated in the circuit

Noise Figure (NF)

$$NF(dB) = SNR_1(dB) - SNR_2(dB)$$

$$= 10\log_{10}\frac{1}{G^2}\frac{P_{noise(output)}}{P_{noise(input)}}$$

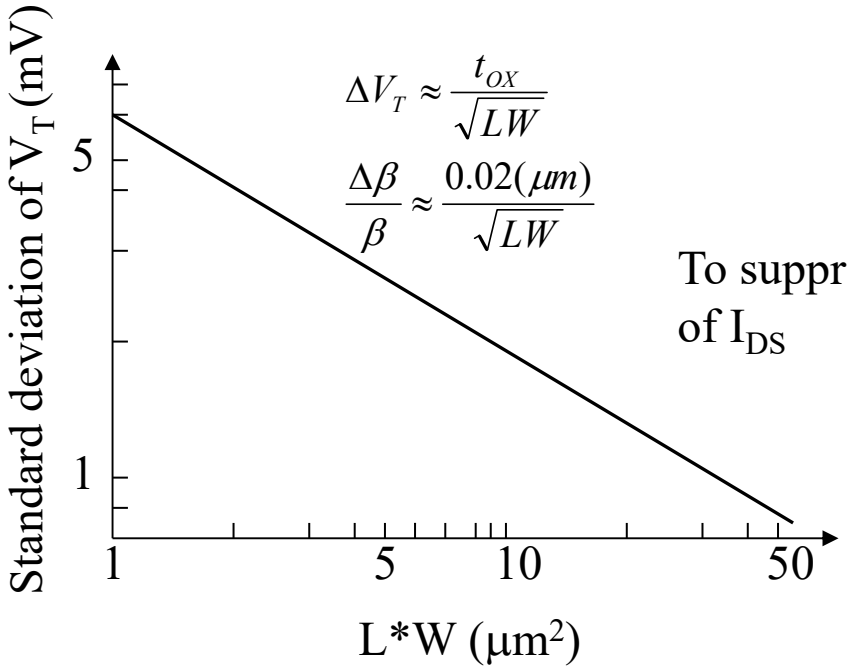


NF depends on the output conductance g_s of signal source. NF is normally measured for $1/g_s = 50(\Omega)$.

7.7 Production tolerance

Fluctuation of circuit characteristics

- The circuit characteristics is sensitive to β and V_T of MOSFET
  - Fluctuation of VT (0.2～10mV in a chip)
    - because of the fluctuation of impurity concentration
  - Fluctuation of β (0.1～5% in a chip)
    - because of the fluctuation of field effect mobility



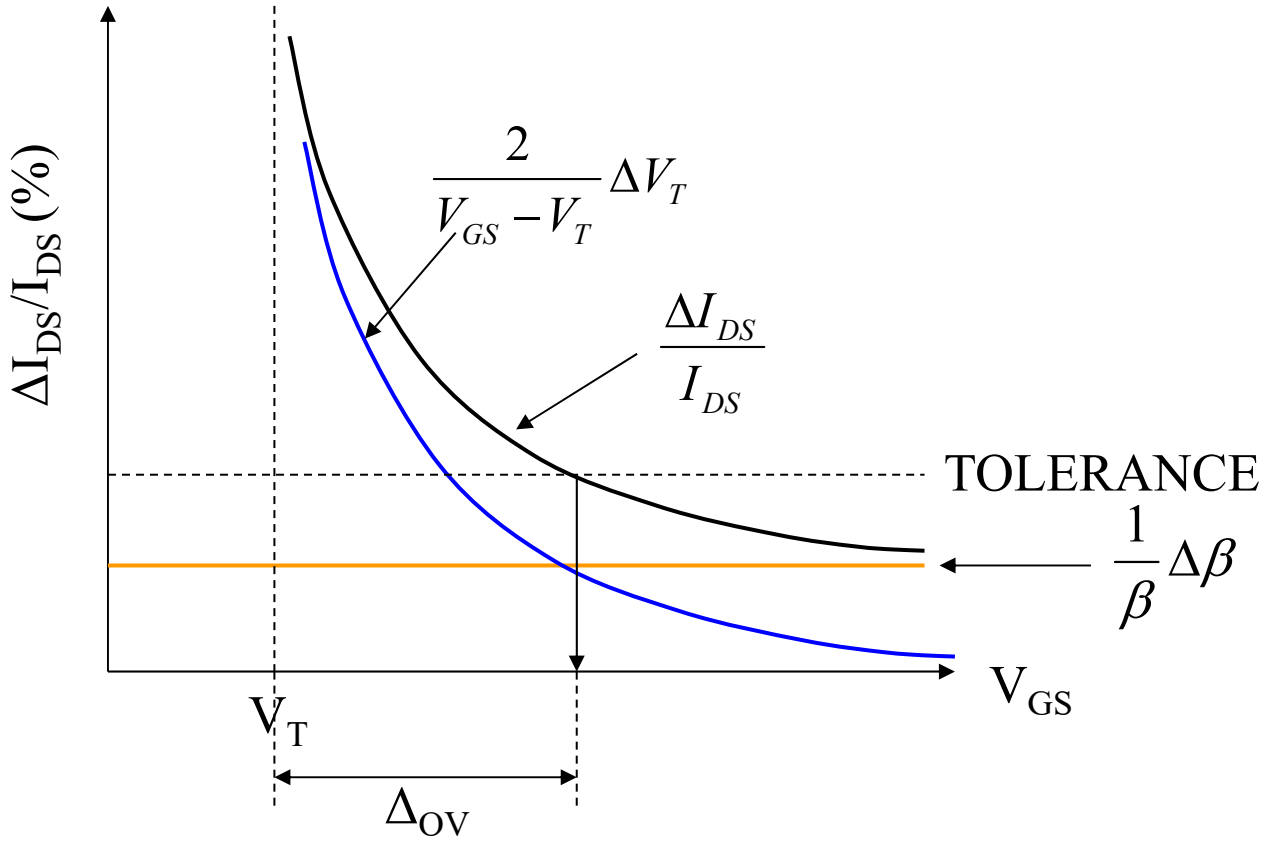
$$I_{DS} = \frac{\beta}{2}(V_{GS} - V_T)^2$$

$$\frac{\Delta I_{DS}}{I_{DS}} = -\frac{2}{V_{GS} - V_T}\Delta V_T + \frac{1}{\beta}\Delta\beta$$

To suppress the fluctuation of I_{DS}

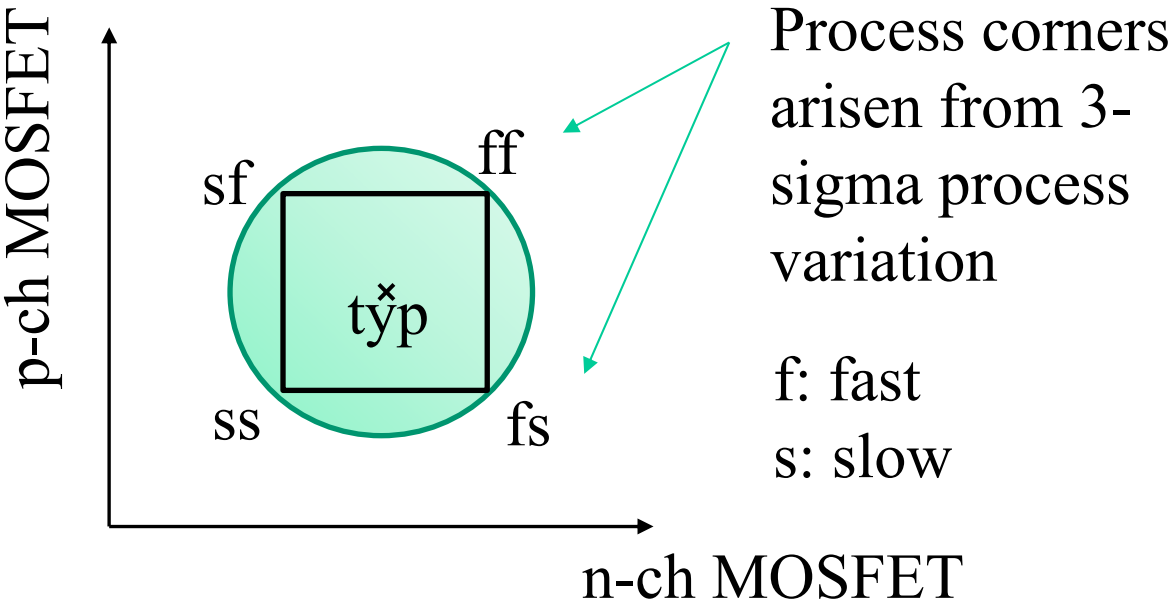
Increase Δ_{OV} = 0.15~0.30
Increase L = 2~5 × L_{min}

Circuit design for the production tolerance



Δ_{OV} is critical for the production tolerance.

Corner Analysis

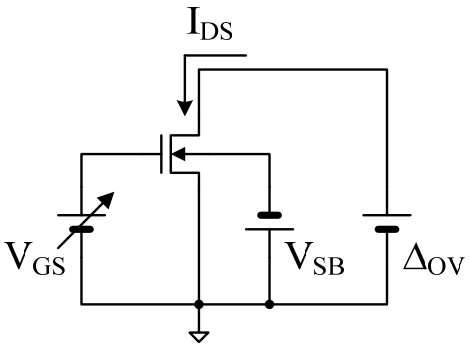


NOTE: The term of corner analysis often means PVT(process, supply voltage and temperature variation) analysis too.

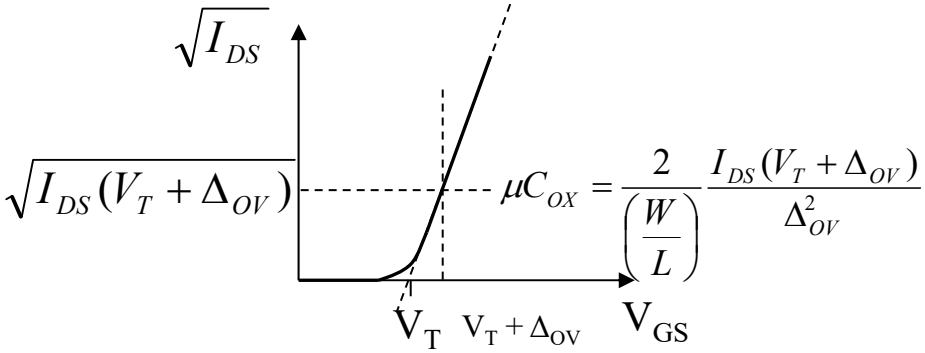
7.8 Parameters for analog design

Parameters of long channel MOSFET for circuit design

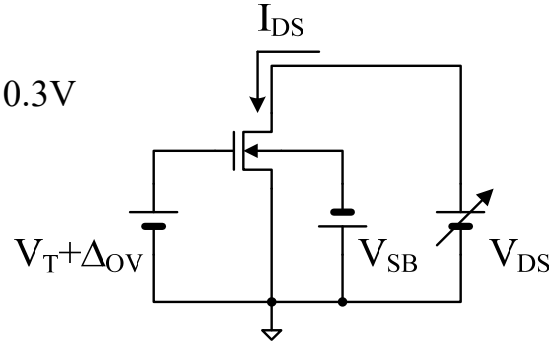
Measurement of V_T and μC_{OX}



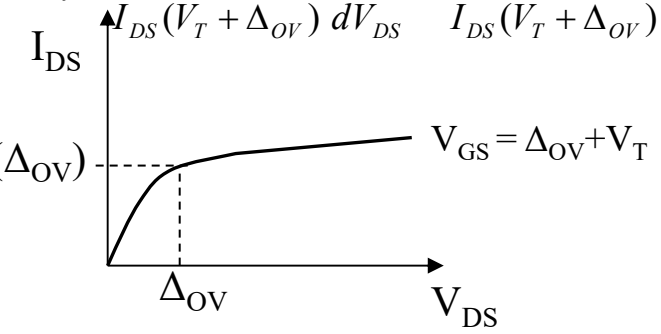
$\Delta_{OV} = 0.15 \sim 0.3V$



Measurement of λ



$$\lambda = \frac{1}{I_{DS}(V_T+\Delta_{OV})}\frac{dI_{DS}}{dV_{DS}} = \frac{g_{ds}}{I_{DS}(V_T+\Delta_{OV})}$$



Saturation condition : $V_{GS} = V_T + \Delta_{OV}$, $V_{DS} = \Delta_{OV}$

NOTE: μC_{OX} is equivalent to Kp of the SPICE parameter.

Summary of MOSFET characteristic

Gate overdrive voltage for bias design

$$\Delta_{OV} = V_{GS} - V_T = \sqrt{\frac{2I_{DS}}{\beta}} = \sqrt{\frac{2I_{DS}}{\mu \cdot C_{OX} \cdot (\frac{W}{L})}}$$

Calculate the suitable value of $I_D/(W/L)$

Transconductance and output conductance for small-signal design

$$g_m = \sqrt{2\beta \cdot I_{DS}}$$

$$g_{ds} = \lambda \cdot I_{DS}$$

Note: The device parameters in analog circuit are specified by the drain current I_{DS}.

Effects of scaling on amplifiers

	$L \rightarrow \frac{L}{\alpha}$
Peak transition frequency:	$f_{T_{peak}} = \frac{v_2}{2\pi L} \propto \alpha$
Voltage gain:	Gain$= \frac{g_m}{r_{ds}} = \frac{\frac{2I_{DS}}{\Delta_{ov}}}{\lambda I_{DS}} = \frac{2}{\lambda \Delta_{ov}} \propto \frac{1}{\alpha}$, *if* Δ_{ov} = *const.*
GBP (Gain bandwidth product):	GBP$= \frac{g_m}{2\pi C_{para}} \propto \alpha$, *if* g_m = *const.*
SNR (Signal to noise ratio):	SNR(Power)$= \frac{v_{sig}^2}{\frac{kT}{C}} \propto \frac{1}{\alpha^2}$, *if* C = *const.*
Power consumption:	$P_{bias} = V_{DD} I_{DS} \propto \frac{1}{\alpha}$, *if* g_m = *const.*

$$P_{bias} = V_{DD} I_{DS} = \frac{V_{DD} g_m \Delta_{ov}}{2} = \frac{\pi kT \Delta_{ov} (SNR)(GBP) V_{DD}}{v_{sig}^2} \propto \alpha \quad , \textit{if GBP and SNR = const.}$$

NOTE: The analytical approach of the amplifier is discussed in later chapters.