3. Modeling of MOSFET for analog design

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# SPICE model of MOSFET

<table>
<thead>
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<th>Feature</th>
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<td>Level 1</td>
<td>Basic physical model ($L &gt; 10,\mu\text{m}$)</td>
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<td>Basic semi-empirical fitting model ($L &gt; 1,\mu\text{m}$), Short-channel effect</td>
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<tr>
<td>BSIM3v3</td>
<td>Berkeley Short-channel IGFET Model, $L &gt; 130,\text{nm}$</td>
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<tr>
<td>BSIM4</td>
<td>$L &lt; 90,\text{nm}$, High frequency</td>
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<td>EKV</td>
<td>Enz-Krummenacher-Vittoz, High precision, Sub-threshold region</td>
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<td>HiSIM</td>
<td>Hiroshima-Univ. STARC IGFET Model, $L &lt; 90,\text{nm}$, High frequency</td>
</tr>
</tbody>
</table>

**BSIM4**: [http://www-device.eecs.berkeley.edu](http://www-device.eecs.berkeley.edu)

```
.model model_name NMOS/PMOS  Level=54
+ vto=0.5  
+ kp=33E-6  model #(The assignment of model depends on the
+ . . . . . circuit simulator.
```
# Model number

<table>
<thead>
<tr>
<th>Model</th>
<th>HSPICE, SmartSpice</th>
<th>Berkeley SPICE</th>
<th>LTspice</th>
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<tr>
<td>Level3</td>
<td>3</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>BSIM3</td>
<td>49/53</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>BSIM4</td>
<td>54</td>
<td>14</td>
<td>14</td>
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<td>BSIMSOI3</td>
<td>57</td>
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<td>EPFL-EKV</td>
<td>55</td>
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</tr>
<tr>
<td>HiSIMHV1.2</td>
<td></td>
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<td>73</td>
</tr>
</tbody>
</table>

NOTE1: Interchange between Spectre and SPICE is possible by using a format indicator for Spectre and SPICE

- `simulator lang = spice` // after here, SPICE format
- `simulator lang = spectre` // after here, Spectre format
(1) DC characteristics of long channel MOSFET
The design parameter of MOSFET is $L$ and $W$.

- **L**: Gate length
- **W**: Gate width
- $L_{\text{eff}}$: Effective channel length
- $W_{\text{eff}}$: Effective channel width
- $x_j$: Junction depth
- $t_{\text{ox}}$: Gate oxide thickness
- $t_{\text{oxf}}$: Field oxide thickness
- $t_m$: poly-Si thickness
L and W of MOSFET

• Analog circuit: Several times larger L than minimum L
  – The production tolerance and mismatch are improved by using larger L.
  – The channel noise in MOSFET is suppressed by using larger L*W.
  – The operating frequency range is decreased by using larger L. (Disadvantage)
  – Very large W/L is required for current drive strength of MOSFET. (Disadvantage)

• Logic circuits: Minimum L
  – The DC transfer characteristic of the logic gate designed only in W/L.
  – The small L achieves a small circuit area.
  – The small L achieves a shot delay time.
Carrier transport mechanism in MOSFET

Weak inversion (Sub-threshold region)

- Exponential I-V
- Diffusion
- Electron Energy
- Distance from source electrode

Strong inversion (Linear and Saturation region)

- Parabolic or linear I-V
- Drift
- Electron Energy
- Distance from source electrode

S(n+)
Channel (p)
D(n+)
$V_{GS}$-$I_{DS}$ Characteristic

- Weak inversion
- Strong inversion

#### Linear (Triode) (1st order)
- $V_{GS} = 0.0V$
- $V_{DS} = 3.3V$

#### Saturation (2nd order)
- $V_{GS} = 1.2V$
- $V_{DS} = 0.6V$

#### Sub-threshold (exponential)
- $V_{GS} = 0.5V$
- $V_{DS} = 0.5V$

n-ch MOSFET

$V_{GS}$ $V_{DS}$ $I_{DS}$
V_{DS}-I_{DS} Characteristic

- Linear (2nd order) \( V_{DS} \leq V_{GS} - V_{Tn} \)
- Saturation (constant) \( V_{DS} \geq V_{GS} - V_{Tn} \)

Sub-threshold

\[ \Delta_{OV} = V_{GS} - V_{Tn} \]

\[ V_{DS} = V_{GS} - V_{Tn} \]

\[ V_{GS} = V_{Tn} \]

n-ch MOSFET

\[ I_{DS} \]

\[ V_{DS} \]
Model equation in linear region

Gradual Channel Approximation

\[ I_{DS} = \frac{W}{L} \mu_n C_{OX} \left\{ (V_{GS} - V_{Tn}) \cdot V_{DS} - \frac{1}{2} V_{DS}^2 \right\} \]

\[ = \beta_n \left\{ (V_{GS} - V_{Tn}) \cdot V_{DS} - \frac{1}{2} V_{DS}^2 \right\} \]

1st order for \( V_{GS} \)  
2nd order for \( V_{DS} \)

\( \mu_n \): Electron mobility \([\text{m}^2/\text{Vs}]\)

\( C_{OX} \): GOX capacitance per area \([\text{F/m}^2]\)

\( V_{Tn} \): Threshold voltage \( \@ \ V_{SB} = 0 \) \([\text{V}]\)
Boundary between linear and saturation region

\[ \frac{dI_{DS}}{dV_{DS}} = \beta_n \{ (V_{GS} - V_{Tn}) - V_{DS} \} = 0 \]

\[ V_{DS} = V_{GS} - V_{Tn} \]
Model equation in saturation region

Gradual Channel Approximation + Boundary equation

\[ V_{DS} = V_{GS} - V_{Tn} \quad // \text{Boundary between linear and saturation region} \]

\[ I_{DS} = \beta_n \{(V_{GS} - V_{Tn}) \cdot (V_{GS} - V_{Tn}) - \frac{1}{2}(V_{GS} - V_{Tn})^2\} \]

\[ = \frac{\beta_n}{2}(V_{GS} - V_{Tn})^2 \]

\{ 2nd order for \( V_{GS} \)  
No dependence on \( V_{DS} \) \}
p-ch and n-ch MOSFET

The n-ch MOSFET and p-ch MOSFET have a complementary characteristics.

\[ V_{DS} = V_{GS} - V_{Tn} \]

\[ V_{DS} = V_{GS} - V_{Tp} \]

\( I_{DS} \): We assume direction flowing into a drain plus.
Chanel length modulation parameter

\[ V_{GS} - V_{DS} \leq V_{Tn} \] (Saturating)

Channel length = \( L_{\text{eff}} - \Delta L \)

(\( \Delta L \) is proportional to \( V_{DS}^{0.5} \))

The drain current increases gradually after saturation, because the channel length is decreasing.

\[ I_{DS} \approx \frac{\beta_n}{2} \left( V_{GS} - V_{Tn} \right)^2 \{1 + \lambda \cdot (V_{DS} - \Delta_{OV})\} \]

Above-mentioned Chanel length parameter (Lambda)
Substrate bias effect

\[ V_{Tn} = V_{FB} + 2 \cdot \phi_B + \frac{1}{C_{OX}} \sqrt{2 \cdot \varepsilon_{Si} \varepsilon_0 \cdot q \cdot N_A (2 \cdot \phi_B - V_{BS})} \]

The \( V_{Tn} \) shifts upwards for \( V_{BS} < 0 \).

Some designer is applying this effect to control the threshold voltage of MOSFET, but the MOSFET cannot operate for \( V_{BS} > 0 \).
Example of simulation result on $V_{Tn}$ shift
Substrate bias in the circuit operation

- The short-circuit with S and B of each transistor prevents substrate bias effect.
- However, the p-well has to be divided, because the well potential of M1 and M2 is different.

No substrate bias          Normal connection

\[ \text{M1} \quad V_{BS} = 0 \quad \text{M2} \quad V_{BS} = 0 \]

\[ \text{M1} \quad V_{BS} < 0 \quad \text{M2} \quad V_{BS} = 0 \]
Sub-threshold Characteristic

Very small current $I_{DS}$ is observed for $V_{GS} < V_{Tn}$

$S$ factor

$$S = \frac{\partial V_{GS}}{\partial \log_{10}(I_{DS})} \equiv S$$

$(\text{log/10 S factor})$
Model equation in sub-threshold region

\[ V_{GS} < V_{Tn} \]

\[ I_{DS} = \frac{W_n}{L_n} I_0 \exp \left\{ \frac{q \cdot (V_{GS} - V_{Tn})}{m \cdot k_B T} \right\} \]

\[ m = 1 + \frac{C_D}{C_{OX}} \]

Exponential for \( V_{GS} \)

\( I_{DS} \) depends on the channel width and temperature.

\( C_{OX} \): GOX capacitance per area

\( C_D \): Capacitance of MOS depletion layer per area
Model equation of n-ch MOSFET

<table>
<thead>
<tr>
<th>$V_{GS}$</th>
<th>$V_{DS}$</th>
<th>$V_{DS} &lt; V_{GS} - V_{Tn}$</th>
<th>$V_{DS} &gt; V_{GS} - V_{Tn}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{GS} &gt; V_{Tn}$</td>
<td>$I_{DS} = \beta_n {(V_{GS} - V_{Tn}) - \frac{1}{2} V_{DS}} V_{DS}$</td>
<td>$I_{DS} = \frac{\beta_n}{2} {V_{GS} - V_{Tn}}^2 {1 + \lambda (V_{DS} - \Delta_{OV})}$ \approx \frac{\beta_n}{2} {V_{GS} - V_{Tn}}^2$ (Saturation)</td>
<td>(Linear)</td>
</tr>
<tr>
<td>$V_{GS} &lt; V_{Tn}$ ($V_{DS} &gt; 0.1V$)</td>
<td>$I_{DS} = \frac{W_n}{L_n} I_0 \exp{\frac{q \cdot (V_{GS} - V_{Tn})}{m \cdot k_{B} T}}$ (Sub-threshold)</td>
<td>$V_{Tn} &gt; 0$ (Enhancement mode)</td>
<td></td>
</tr>
</tbody>
</table>

$\beta_n = \frac{W_n}{L_n} \mu_n C_{OX}$ \quad $m = 1 + \frac{C_D}{C_{OX}}$

$C_{OX} = \varepsilon_0 \varepsilon_{SiO_2} \frac{1}{t_{OX}}$

$C_{OX}$: GOX capacitance per area (F/m²) \quad $\mu_n$: Field effect mobility of electron (m²/Vsec)
### Model equation of p-ch MOSFET

<table>
<thead>
<tr>
<th>V&lt;sub&gt;GS&lt;/sub&gt;</th>
<th>V&lt;sub&gt;DS&lt;/sub&gt;</th>
<th>V&lt;sub&gt;DS&lt;/sub&gt; &gt; V&lt;sub&gt;GS&lt;/sub&gt; - V&lt;sub&gt;Tp&lt;/sub&gt;</th>
<th>V&lt;sub&gt;DS&lt;/sub&gt; &lt; V&lt;sub&gt;GS&lt;/sub&gt; - V&lt;sub&gt;Tp&lt;/sub&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;GS&lt;/sub&gt; &lt; V&lt;sub&gt;Tp&lt;/sub&gt;</td>
<td>[ I_{DS} = -\beta_p \left((V_{GS} - V_{Tp}) - \frac{1}{2} V_{DS}\right) V_{DS} ] (Linear)</td>
<td>[ I_{DS} = \frac{-\beta_p}{2} (V_{GS} - V_{Tp})^2 {1 + \lambda (V_{DS} - \Delta_{OV})} ] (Saturation)</td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;GS&lt;/sub&gt; &gt; V&lt;sub&gt;Tp&lt;/sub&gt; (V&lt;sub&gt;DS&lt;/sub&gt; &lt; 0.1V)</td>
<td>[ I_{DS} = -\frac{W_p}{L_p} I_0 \exp\left{\frac{q \cdot (V_{GS} - V_{Tp})}{m \cdot k_B T}\right} ] (Sub-threshold)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\[ \beta_p = \frac{W_p}{L_p} \mu_p \cdot C_{OX} \] \[ m = 1 + \frac{C_D}{C_{OX}} \]

\[ C_{OX} = \varepsilon_0 \varepsilon_{SiO_2} \frac{1}{t_{OX}} \]

- \( \beta_p \): GOX capacitance per area (F/m\(^2\))
- \( \mu_p \): Field effect mobility of hole (m\(^2\)/V/sec)
- \( C_{OX} \): GOX capacitance per area (F/m\(^2\))
- \( m \): Enhancement factor
- \( \Delta_{OV} \): Overvoltage
- \( V_{DS} \): Drain to Source voltage
- \( V_{GS} \): Gate to Source voltage
- \( V_{Tp} \): Threshold voltage
- \( \Delta_{OV} \): Overvoltage
- \( I_{DS} \): Drain to Source current
- \( I_0 \): Saturation current
- \( W_p \): Channel width
- \( L_p \): Channel length
- \( C_D \): Channel capacitance
- \( k_B T \): Boltzmann constant times temperature

\[ V_{Tp} < 0 \] (Enhancement mode)
Gate overdrive voltage $\Delta_{OV}$

Saturation condition: $V_{DS} > V_{GS} - V_T = \Delta_{OV}$

$$
\Delta_{OV} = V_{GS} - V_T = \sqrt{\frac{2I_{DS}}{\beta}} = \sqrt{\frac{2I_{DS}}{\mu \cdot C_{OX} \cdot \left(\frac{W}{L}\right)}}
$$

$(W/L) = \text{const.}$

$I_{DS} = \text{const.}$
(2) DC characteristics of short channel MOSFET
Influence of scaling down to L < 0.3μm

- **Short channel effect**
  - The threshold voltage $V_T$ is decreased with decreasing L.
    - The three-dimensional distribution of the electric field in the MOSFET depends on an aspect ratio of cross section.
  - The $I_{DS}$-$V_{GS}$ curve shows the linear characteristic in the saturation region and the boundary of linear and saturation region is obscured.
    - The strength of electric field in the channel is very high and the electron veracity in the channel is saturated.
  - The leak current of the sub-threshold region is increased.
    - The $V_{DS}$ contributes the generation of the channel, and the tunneling current is increased with increasing the electric field of drain edge.

The simulation model considering to the short channel effect have to be used.
$L$-dependence of $V_T$

The fluctuation of $V_T$ is sensitive to the fluctuation of $L$ of the short channel MOSFET.

The amount of the charge controlled by $V_{GS}$ is decreased with decreasing $L$.

The impurity concentration in channel is equivalently decreased and $V_T$ is lowered.
Saturation of the drift velocity

Low electric field: Proportional to the strength of the electric field
High electric field: Saturated for the strength of the electric field

\[ I_{DS} = \frac{\beta_n}{2} \left(V_{GS} - V_{Tn}\right)^2 \]

\[ \beta_n = \frac{W_n}{L_n} \mu_n C_{OX} \]

| \( v_n \) | = \( \mu_n \cdot |E| \) (low E)

| \( v_n \) | = \( v_{sat} \) (high E)
Degradation of S factor

- Decreasing Threshold Voltage
- Increasing Sub-threshold (Cut-off) Current
Characteristics of Short channel MOSFET

Long Channel MOSFET

\[ I_{DS} = \frac{\beta_n}{2} (V_{GS} - V_{Tn})^2 \{1 + \lambda(V_{DS} - \Delta_{OV})\} \]

Short Channel MOSFET

\[ I_{DS} = W_n \cdot \nu_{sat} \cdot C_{OX} (V_{GS} - V_{Tn}) \{1 + \lambda(V_{DS} - \Delta_{OV})\} \]

\( \nu_{sat} \): Saturation velocity of the carrier
(3) Capacitance-Voltage (C-V) characteristics
Parasitic capacitance in MOSFET

Overlap Capacitance between G-D and G-S (constant)

Capacitance between G-B (depending on the bias voltage)

p+ n+ n+ SG D

Cross section

C_{OV} C_{GB}

C_{PN} L_{OV} L_{D}

pn junction capacitance of D and S layer (depending on the bias voltage)
Bias dependence of pn junction capacitance ($C_{PN}$) -1

The width of depletion layer depends on the bias voltage.

The ionized donor and acceptor works as an electric double layer capacitor.

Potential $V$

Depletion layer

Forward bias $V_B - V_{PN}$
Zero bias $V_B$
Reverse bias $V_B + V_{PN}$

Position $x$

The width of depletion layer depends on the bias voltage.
Bias dependence of pn junction capacitance ($C_{PN}$) -2

Model equation of C-V characteristic

$$C_{PN} = \varepsilon_0 \varepsilon_S \frac{S}{d}$$

Junction area

$\text{Depletion layer width}$

$$= \frac{C_{PN}(0V)}{\sqrt{1 - \frac{V_{PN}}{V_B}}}$$

$V_B$: Built-in Potential $\sim 0.6 \sim 0.9V$

NOTE: This equation is obtained according to depletion layer capacitance, and cannot be applicable to estimate the forward bias capacitance, because the injected minority carrier play a roll of a electric double layer capacitor (usually large value) in the high-level injection condition.
Bias dependence of MOS (C_{MOS}) -1

Electron energy lineup of the strong inversion for p-substrate MOS for V_{GB} > V_{Th}

\[ V_{GB} = V_{OX} + \phi_S \]

- $C_{OX}$: GOX capacitance per area
- $C_S$: Depletion layer capacitance per area

\[ \phi_S = \frac{C_{OX}}{C_{OX} + C_S} \]

Equivalent circuit
Bias dependence of MOS ($C_{MOS}$) -2

In the weak inversion for p-substrate MOS for $V_{GB} < V_{Tn}$

Depletion layer and GOX capacitance per area

$$C_S = \frac{\varepsilon_0 \varepsilon_{Si}}{x_D}$$

$$C_{OX} = \frac{\varepsilon_0 \varepsilon_{SiO_2}}{t_{OX}}$$

Total capacitance

$$C_{MOS} = \frac{1}{\frac{1}{C_{OX}} + \frac{1}{C_S}}$$

Width of depletion layer

$$x_D = \sqrt{\frac{2\varepsilon_0 \varepsilon_{Si} \phi_S}{qN_A}}$$

$$\phi_S = \frac{C_{OX}}{C_{OX} + C_S} V_{GB}$$
Bias dependence of MOS ($C_{MOS}$) -3

C-V characteristic of MOS capacitor

$$C_{MOS} \approx C_{OX}$$

$$C_{MOS} = \frac{1}{\frac{1}{C_{OX}} + \frac{1}{C_s(V_{GB})}}$$

The depletion layer width cannot grow anymore with increasing $V_{GB}$ in the strong inversion condition, and $C_s$ is fixed at $C_s(V_{Tn})$.

$$C_{GS} = C_{OX}$$

$$C_{MOS} = \frac{1}{\frac{1}{C_{OX}} + \frac{1}{C_s(V_{Tn})}}$$
Interelectrode capacitance of MOSFET

\[ C_{gs} = C_{ov} + \alpha(V) \cdot C_{OX} \]

The variable \( \alpha(V) \) depends on the bias condition. \( \alpha(V) \approx 2/3 \) in the strong inversion condition (linear region and saturation region).

\[ C_{ds} = C_{j} \]

\[ C_j(V) = \frac{C_j(0)}{\sqrt{2^{-3/2} + \frac{V}{2\phi_B}}} \]
Model of interelectrode capacitance

Capacitance independent on bias
CGDO: G-D overlap capacitance
CGSO: G-S overlap capacitance
CGBO: G-B overlap capacitance

<table>
<thead>
<tr>
<th>Label</th>
<th>Sub-threshold region</th>
<th>Linear region</th>
<th>Saturation region</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{GD}$</td>
<td>CGDO*W</td>
<td>0.5*C_{OX}<em>W</em>L</td>
<td>CGDO*W</td>
</tr>
<tr>
<td>$C_{DB}$</td>
<td>C_{j}<em>W</em>L_{D}</td>
<td>C_{j}<em>W</em>L_{D}</td>
<td>C_{j}<em>W</em>L_{D}</td>
</tr>
<tr>
<td>$C_{GB}$</td>
<td>C_{OX}<em>W</em>L_{eff}</td>
<td>CGBO*L</td>
<td>CGBO*L</td>
</tr>
<tr>
<td>$C_{GS}$</td>
<td>CGSO*W</td>
<td>0.5*C_{OX}<em>W</em>L</td>
<td>2/3*C_{OX}<em>W</em>L</td>
</tr>
<tr>
<td>$C_{SB}$</td>
<td>C_{j}<em>W</em>L_{S}</td>
<td>C_{j}<em>W</em>L_{S}</td>
<td>C_{j}<em>W</em>L_{S}</td>
</tr>
</tbody>
</table>
(4) AC characteristics
Biasing for MOSFET operation

• Analog circuit operates with biasing
  – The DC bias is applied to perform
  – The MOSFETs are operated in the saturation region and sometimes in the linear region and sub-threshold region if needed.
  – The small-signal parameters are depends on the bias current $I_{DS}$ in the saturation region.
  – The bias current $I_{DS}$ is designed with the circuit parameter $V_{GS}$ and $W/L$.

• Digital circuit does not require the idea of biasing
  – Logic value '1' ← Linear(p-ch), Sub-threshold(n-ch)
  – Logic value '0' ← Linear(n-ch), Sub-threshold(p-ch)
  – '1' $\iff$ '0' transition = Saturation region(p-ch and n-ch)
Transconductance $g_m - 1$

The transconductance $g_m$ expresses ability for amplification of the MOSFET.

$$\frac{\partial I_{DS}}{\partial V_{GS}}\bigg|_{I_{DS}}$$

NOTE: Small-signal parameters of p-ch and n-ch MOSFET are given by the same expression, because the small-signal parameters connected to the slope of the DC characteristics.
Transconductance $g_m$ -2

Bias current dependence of $g_m$

**$V_{GS} < V_{Tn}$ (Sub-threshold region)**

$$I_{DS} = \frac{W_n}{L_n} I_0 \exp\left\{ \frac{q \cdot (V_{GS} - V_{Tn})}{m \cdot k_B T} \right\}$$

$$g_m = \frac{W_n}{L_n} \frac{q}{m \cdot k_B T} \exp\left\{ \frac{q \cdot (V_{GS} - V_{Tn})}{m \cdot k_B T} \right\} = \frac{q \cdot I_{DS}}{m \cdot k_B T}$$

**$V_{GS} > V_{Tn}$ (Saturation region)**

Long Channel ($E_{sat} \cdot L >> V_{GS} - V_{Tn}$)

$$I_{DS} = \frac{\beta_n}{2} (V_{GS} - V_{Tn})^2$$

$$g_m = \beta_n (V_{GS} - V_{Tn}) = \sqrt{2} \beta_n \cdot I_{DS}$$

$$g_m = \frac{2I_{DS}}{V_{GS} - V_{Tn}}$$

Short Channel ($E_{sat} \cdot L < V_{GS} - V_{Tn}$)

$$I_{DS} = v_{sat} WC_{OX} (V_{GS} - V_{Tn})$$

$$g_m = v_{sat} WC_{OX}$$
Transconductance $g_m$ - 3

Circuit performance depending on $\Delta_{OV}$

Gain/power ratio

$$I_{DS} = \frac{\beta_n}{2} (V_{GS} - V_{Tn})^2 = \frac{\beta_n}{2} \Delta_{OV}$$

$$\Delta_{OV} = \sqrt{\frac{2I_{DS}}{\beta_n}}$$

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \beta_n \cdot \Delta_{OV}$$

$$\frac{g_m}{I_{DS}} = \frac{2}{\Delta_{OV}} \quad \text{Small $\Delta_{OV}$ is better.}$$

Sensitivity for $V_T$ fluctuation

$$\frac{\partial I_{DS}}{\partial V_{Tn}} = -\Delta_{OV}$$

$$\frac{\partial I_{DS}}{I_{DS}} = -\beta_n \cdot \Delta_{OV} \quad \frac{\partial V_{Tn}}{I_{DS}} = -\frac{2\partial V_{Tn}}{\Delta_{OV}}$$

Large $\Delta_{OV}$ is better.
Bias current dependence of $g_m$

The previous equations are simplified assuming $m = 1$. The parameter $m$ is derived from the dependence of $C_d$ on $V_{GS}$.
Optimization of $\Delta_{OV}$

- $\Delta_{OV}$ depends on $W/L$, and $I_{DS}$.
- $g_m$ and the production tolerance depends on $\Delta_{OV}$. Therefore, there is a reasonable range in a value of $\Delta_{OV}$.
- The value of $V_{GS}$ is usually chosen among the range of $\Delta_{OV} = 0.15V \sim 0.30V$

Typically $\Delta_{OV} = 0.2V$

\[ V_{GS} = V_T + \Delta_{OV} \]
Output conductance $g_{ds}$

$g_{ds}$ in saturation region

$$I_{DS} = \frac{\beta_n}{2} (V_{GS} - V_{Tn})^2 \{1 + \lambda(V_{DS} - \Delta_{OV})\}$$

$$y_{22} = g_{ds} = \frac{\partial I_{DS}}{\partial V_{DS}} = \frac{\beta_n}{2} (V_{GS} - V_{Tn})^2 \cdot \lambda$$

$$\cong \lambda \cdot I_{DS} \quad (V_{DS} > V_{GS} - V_{Tn})$$

$g_{ds}$ in linear region

$$I_{DS} = \beta_n \{V_{GS} - V_{Tn}\} \cdot V_{DS} - \frac{1}{2} V_{DS}^2$$

$$y_{22} = g_{ds} = \frac{\partial I_{DS}}{\partial V_{DS}} = \beta_n \{V_{GS} - V_{Tn}\} - V_{DS} \quad (V_{DS} < V_{GS} - V_{Tn})$$
$y$ parameters of MOSFET

Small-signal equivalent circuit

\[
\begin{bmatrix}
i_{gs} \\
i_{ds}
\end{bmatrix} =
\begin{bmatrix}
y_{11} & y_{12} \\
y_{21} & y_{22}
\end{bmatrix}
\begin{bmatrix}
v_{gs} \\
v_{ds}
\end{bmatrix}
\]

\[
y_{11} y_{12} =
\begin{bmatrix}
j \omega \cdot C_{gs} & 0 \\
g_m & g_{ds}
\end{bmatrix}
\]

Small-signal equivalent circuit (C_{gs} includes C_{gb})

\[
g_m = \sqrt{2 \beta_n I_{DS}}
\]

\[
g_{ds} = \lambda_n I_{DS}
\]

Simplified equivalent circuit

(C_{gs} >> C_{gd} in a saturation region)
h parameters of MOSFET

\[
\begin{align*}
\begin{bmatrix}
    v_1 \\
    i_2
\end{bmatrix}
&= 
\begin{bmatrix}
    h_{11} & h_{12} \\
    h_{21} & h_{22}
\end{bmatrix}
\begin{bmatrix}
    i_1 \\
    v_2
\end{bmatrix}
\begin{bmatrix}
    1 \\
    j \omega \cdot C_{gs}
\end{bmatrix}
\begin{bmatrix}
    g_m \\
    j \omega \cdot C_{gs}
\end{bmatrix}
\begin{bmatrix}
    0 \\
    g_{ds}
\end{bmatrix}
\end{align*}
\]

\[h_{21} = \left. \frac{i_2}{i_1} \right|_{v_2=0} = \frac{g_m}{j \omega \cdot C_{gs}}\]

\[
\begin{align*}
\begin{cases}
    i_1 = j \omega \cdot C_{gs} \cdot v_1 \\
    i_2 = g_m \cdot v_1 \\
    (v_2 = 0)
\end{cases}
\end{align*}
\]

Transition Frequency

\[f_T = \frac{g_m}{2 \pi \cdot C_{gs}}\]

when \( f = f_T, \ |h_{21}| = 1 \) (= 0dB)

where \( g_m \) depends on \( W/L \) and \( I_{DS} \) (long channel)
Transition Frequency $f_T$

The frequency for the current gain $h_{21} = 1$

**Long channel MOS**

$$I_{DS} = \frac{\beta}{2} (V_{GS} - V_T)^2$$

$$\beta = \mu \cdot C_{OX} \cdot \frac{W}{L}$$

$$g_m = \frac{dI_{DS}}{dV_{GS}} = \sqrt{2\beta \cdot I_{DS}}$$

$$f_T = \frac{\sqrt{2\beta \cdot I_{DS}}}{2\pi \cdot C_{gs}}$$

depending on the bias current

**Short channel MOS**

$$I_{DS} = v_{SAT} C_{OX} W (V_{GS} - V_T)$$

$$g_m = \frac{dI_{DS}}{dV_{GS}} = v_{SAT} C_{OX} W$$

$$f_{T\_peak} = \frac{v_{SAT} C_{OX} W}{2\pi \cdot C_{gs}} = \frac{v_{SAT} C_{OX} W}{2\pi \cdot C_{OX} W \cdot L} = \frac{v_{SAT}}{2\pi \cdot L}$$

independent on the bias

[Ref.] $g_m$ of bipolar junction transistor (BJT)

$$I_B = I_S (e^{qV_{BE}/kT} - 1)$$

$$\frac{dI_B}{dV_{BE}} \approx \frac{q}{kT} I_B$$

$$g_m = \frac{dI_C}{dV_{BE}} = \frac{dI_B}{dV_{BE}} \frac{dI_C}{dI_B} \approx \frac{q}{kT} I_B \cdot h_{fe} = \frac{q}{kT} I_C$$
RF and mixed signal technology trend

- Bipolar (priority=speed)
- CMOS (priority=Low Standby Power)
- Bipolar (Normal)
- CMOS (priority=precision)
- Bipolar (priority=high voltage, for RF power amp.)
(5) Inherent noise
Quantification of the noise

PSD: Power Spectrum Density of noise

\[ PSD = v_{\text{noise}}^2 (f) \]  \hspace{1cm} \text{(V}^2/\text{Hz)}

RMS noise voltage in the band from \( f_L \) to \( f_H \)

\[ \sqrt{\int_{f_L}^{f_H} v_{\text{noise}}^2 (f) \cdot df} \]  \hspace{1cm} \text{(V)}

RMS noise power in the band from \( f_L \) to \( f_H \)

\[ \frac{1}{R} \int_{f_L}^{f_H} v_{\text{noise}}^2 (f) \cdot df \]  \hspace{1cm} \text{(W)}
Source of inherent noise

1. Thermal noise (Johnson noise)
   - Random movement of carrier in all conductive material
   - White noise
   - independent on the bias

2. Flicker noise
   - Random ionization of deep level trap in semiconductors
   - $1/f$ noise ($1/f^n$, where $n=0.8 \sim 1.3$)
   - dependent on the bias
   - inversely proportional to $L*W$ of MOSFET

3. Shot noise (modeled after BSIM4)
   - Statistical fluctuation of thermal emission and tunneling through the potential barrier in semiconductors
   - White noise
   - proportional to voltage
   - observed in the short channel MOSFET ($t_{ox} < 20$nm)
Thermal noise of resistor

\[ i_{\text{noise}} = \frac{4kT}{R} \text{ (A}^2\text{/Hz)} \]

\[ v_{\text{noise}} = 4kTR \text{ (V}^2\text{/Hz)} \]
Thermal noise of RC circuit

\[ v_{out} = \frac{1}{1 + j\omega CR}, \quad v_{noise} = \frac{1}{1 + j\omega/\omega_p}, \quad \omega_p = \frac{1}{CR} \]

\[ \overline{v_{out}^2} = \frac{\overline{v_{noise}^2}}{1 + \omega^2/\omega_p^2} \]

\[ RMS(v_{out}^2) = \sqrt{\int_0^\infty v_{out}^2 \, d\omega} = \sqrt{\frac{kT}{C}} \]

Large C suppresses the thermal noise generated by the resistor, but the time constant of the circuit is increased.

NOTE: The RMS of thermal noise \( v_{out} \) is limited by the size of the capacitor, and independent of the size of the resistor.
Thermal noise of MOSFET

PSD of the thermal noise depends on the conductance.

\[
\frac{i^2}{2} = 4k_BT\gamma \cdot \frac{2}{3} g_m \quad \text{(Saturation region)}
\]

\[
\frac{v^2}{2} = \frac{i^2}{2
\]

\[
= \frac{8k_BT\gamma}{3g_m}
\]

\[
\gamma = 1 \quad \text{(Long Channel > 0.25\mu m)}
\]

\[
\gamma = 2 \quad \text{(Short Channel < 0.25\mu m)}
\]

Normally this equation is used.
Limitation of the gate width

PSD of the gate resistance noise

\[ \nu_{\text{noise}}^2 = 4k_B T \cdot R_G = 4k_B T \cdot R_{\square \text{g}} \frac{W}{L} \]

PSD of the channel resistance noise

\[ \nu_{\text{noise}}^2 = \frac{8k_B T \cdot \gamma}{3g_m} \]

W/L is limited according to the thermal noise condition:
Gate resistance noise < Channel resistance

\[ R_{\square \text{g}} \frac{W}{L} \leq \frac{2}{3 \gamma} \frac{\gamma}{3g_m} \approx \frac{1}{g_m} \]
Flicker noise of MOSFET

PSD of the Flicker noise depends on the L*W.

\[
\overline{v^2_{\text{noise}}} = \frac{K_F}{C_{OX}^2 W \cdot L} \frac{1}{f^n}
\]

\[K_F \approx 10^{-24} \ (V^2 F) \ (n\text{-ch})\]

\[\approx 10^{-25} \ (V^2 F) \ (p\text{-ch})\]

\[n \approx 0.8 \sim 1.3\]

Designed depending on the process

Quantized Flicker noise of Ultra-narrow-W MOSFET
PSD of dominant noise in MOSFET

- The 1/f noise is an intrinsic noise in semiconductors.
- The thermal noise occurs anywhere in conductor.

The bandwidth of the circuit $\Delta f$ should be limited to a signal band.

Effective noise voltage $= \sqrt{v_{noise}^2 \cdot \Delta f}$

The diagram illustrates the PSD of noise contributions, with 1/f noise and thermal noise bands. The bandwidth $\Delta f$ is notable around ~1 MHz.
SNR and NF

Noise strength mixed in the signal

SNR: Signal to Noise Ratio

Noise voltage

\[
SNR(dB) = 20 \log_{10} \left| \frac{V_{signal}}{V_{noise}} \right|
\]

Noise power

\[
SNR(dB) = 10 \log_{10} \left| \frac{P_{signal}}{P_{noise}} \right|
\]

NOTE: The absolute noise strength is often given by the input-referred noise power (dBm).

Noise strength generated in the circuit

Noise Figure (NF)

\[
NF(dB) = SNR_1(dB) - SNR_2(dB)
\]

\[
= 10 \log_{10} \left( \frac{1}{G^2} \frac{P_{noise(output)}}{P_{noise(input)}} \right)
\]

NF depends on the output conductance \( g_s \) of signal source. NF is normally measured for \( 1/g_s = 50(\Omega) \).
(6) Production tolerance
Fluctuation of circuit characteristics

- The circuit characteristics is sensitive to $\beta$ and $V_T$ of MOSFET
  - Fluctuation of $V_T$ (0.2～10mV in a chip)
    - because of the fluctuation of impurity concentration
  - Fluctuation of $\beta$ (0.1～5% in a chip)
    - because of the fluctuation of field effect mobility

$$\Delta V_T \approx \frac{t_{ox}}{\sqrt{LW}}$$
$$\frac{\Delta \beta}{\beta} \approx \frac{0.02(\mu m)}{\sqrt{LW}}$$

$$I_{DS} = \frac{\beta}{2} (V_{GS} - V_T)^2$$

$$\frac{\Delta I_{DS}}{I_{DS}} = -\frac{2}{V_{GS} - V_T} \Delta V_T + \frac{1}{\beta} \Delta \beta$$

To suppress the fluctuation of $I_{DS}$

To increase $\Delta_OV = 0.15\sim 0.3$

Increase $L = 2\sim 5 \times L_{\text{min}}$
Circuit design for the production tolerance

\[ \Delta I_{\text{DS}} / I_{\text{DS}} (\%) = \frac{2}{V_{\text{GS}} - V_T} \Delta V_T \]

\[ \frac{\Delta I_{\text{DS}}}{I_{\text{DS}}} \]

\[ \frac{1}{\beta} \Delta \beta \]

\[ \Delta_{\text{OV}} \]

\[ V_T \]

\[ V_{\text{GS}} \]

\[ \Delta_{\text{OV}} \text{ is critical for the production tolerance.} \]
Corner Analysis

Process corners arisen from 3-sigma process variation

f: fast
s: slow

NOTE: The term of corner analysis often means PVT (process, supply voltage and temperature variation) analysis too.
(7) Design parameters
Parameters of long channel MOSFET for circuit design

Measurement of $V_T$ and $\mu C_{OX}$

\[
\sqrt{I_{DS}}(V_T + \Delta_{OV}) \quad \mu C_{ox} = \frac{2 \cdot I_{ds}(V_T + \Delta_{ov})}{W \cdot L} \quad V_{GS} = V_T + \Delta_{OV} \quad \Delta_{OV} = 0.15 \sim 0.3V
\]

Saturation condition : $V_{GS} = V_T + \Delta_{OV}, V_{DS} = \Delta_{OV}$

NOTE: $\mu C_{OX}$ is equivalent to $Kp$ of the SPICE parameter.

Measurement of $\lambda$

\[
\lambda = \frac{1}{I_{DS}(V_T + \Delta_{OV})} \frac{dI_{DS}}{dV_{DS}} = \frac{g_{ds}}{I_{DS}(V_T + \Delta_{OV})}
\]

$V_{GS} = \Delta_{OV} + V_T$
(8) Scaling of analog circuits
Effects of scaling on amplifiers

\[ L \rightarrow \frac{L}{\alpha} \]

Peak transition frequency:

\[ f_{\text{peak}} = \frac{v_2}{2\pi L} \propto \alpha \]

Voltage gain:

\[ \text{Gain} = \frac{g_m}{r_{ds}} = \frac{2I_{DS}}{\lambda I_{DS}} = \frac{2}{\lambda \Delta_{ov}} \propto \frac{1}{\alpha}, \text{ if } \Delta_{ov} = \text{const.} \]

GBP (Gain bandwidth product):

\[ \text{GBP} = \frac{g_m}{2\pi C_{\text{para}}} \propto \alpha, \text{ if } g_m = \text{const.} \]

SNR (Signal to noise ratio):

\[ \text{SNR}(\text{Power}) = \frac{v_{\text{sig}}^2}{kT} \propto \frac{1}{\alpha^2}, \text{ if } C = \text{const.} \]

Power consumption:

\[ P_{\text{bias}} = V_{DD}I_{DS} \propto \frac{1}{\alpha}, \text{ if } g_m = \text{const.} \]

\[ P_{\text{bias}} = V_{DD}I_{DS} = \frac{V_{DD}g_m\Delta_{ov}}{2} = \frac{\pi kT \Delta_{ov}(\text{SNR})(\text{GBP})V_{DD}}{v_{\text{sig}}^2} \propto \alpha, \text{ if } \text{GBP and SNR} = \text{const.} \]

NOTE: The analytical approach of the amplifier is discussed in later chapters.
Summary of MOSFET characteristic

Gate overdrive voltage for bias design

$$\Delta_{OV} = V_{GS} - V_T = \sqrt{\frac{2I_{DS}}{\beta}} = \sqrt{\frac{2I_{DS}}{\mu \cdot C_{OX} \cdot \left(\frac{W}{L}\right)}}$$

Calculate the suitable value of $I_D/(W/L)$

Transconductance and output conductance for small-signal design

$$g_m = \sqrt{2\beta \cdot I_{DS}}$$

$$g_{ds} = \lambda \cdot I_{DS}$$

Note: The device parameters in analog circuit are specified by the drain current $I_{DS}$. 