12. Single-end operational amplifier

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12.1 Specification of OPA

Parameters of OPA

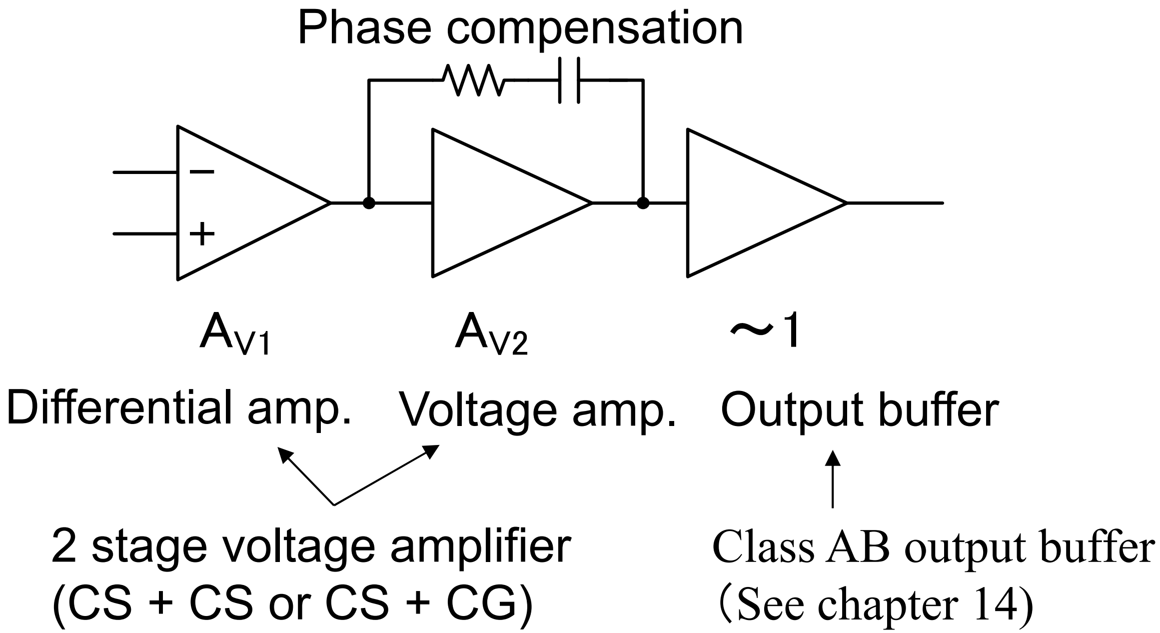
Parameter	Design constraint	Description
VDD (V)	max/typ/min	Power supply voltage
I_{Bias} (uA)	max	Total bias current
Open loop gain A_d (dB)	min	Differential gain
Sampling frequency f_S (Hz)	max	For discrete CMFB OPA
GBP (Hz)	min	Unity gain frequency
SR (V/us)	min	>> 2*VDD/f_S
Settling time (us)	max	< 2/fs
Phase margin (deg)	min	> 60 deg.
Common-mode input range (V)	min/max	
Output swing (V)	min/max	> Differential input range
Input-referred noise level (uV @Hz)	max	In frequency range
Input-referred offset V_{OS} (V)	max	
CMRR (dB)	min	Common Mode Rejection Ratio
PSRR (dB)	min	Power Supply Rejection Ratio
Load resistance, capacitance (ohm, F)	typ	Possible external load

Sample Format of specification sheet

Parameter		Target value	Simulation			Measured value			Unit	Comment
			min.	typ.	max.	min.	typ.	max.		
VDD		1.8							V	
Bias current		312							uA	No input
Open loop gain		82							dB	
GBP		320M							Hz	Load=100fF
SR		244							V/us	Load=100fF
Settling time		24n							us	Error 1%
CMRR		-185							dB	
PSRR		-150							dB	
Noise level		50							$nV/Hz^{0.5}$	@1MHz
Common-mode input range	upper	-0.5							V	
	lower	0.9							V	

Estimated from the host system of the circuit

Circuit configuration of OPA



Phase compensation

−

+

A_{V1} A_{V2} ～1

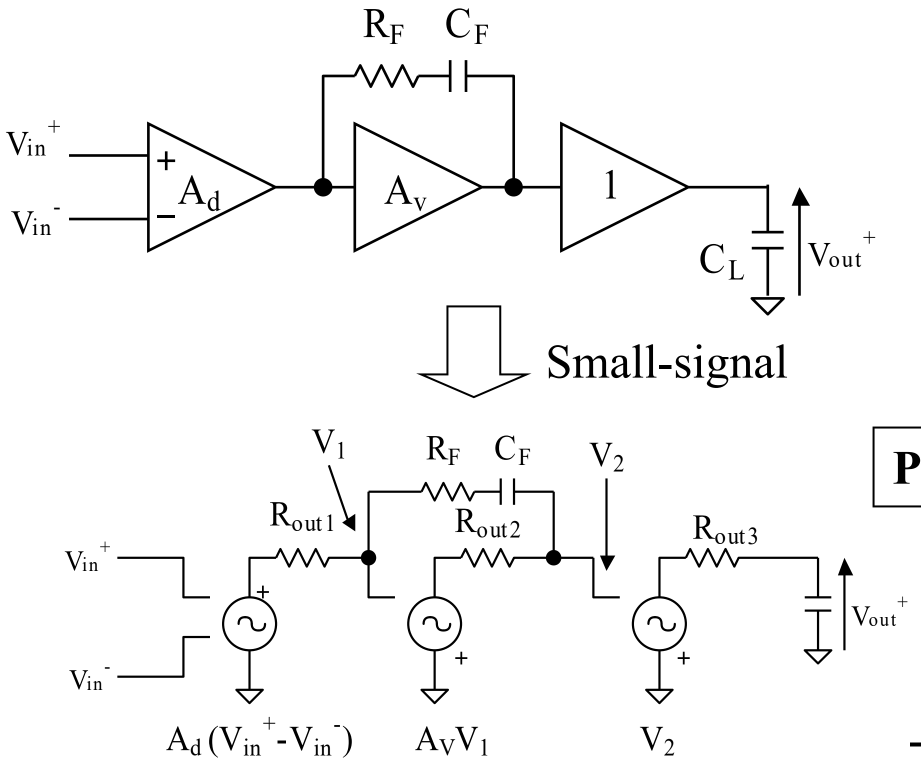
Differential amp. Voltage amp. Output buffer

2 stage voltage amplifier
(CS + CS or CS + CG)

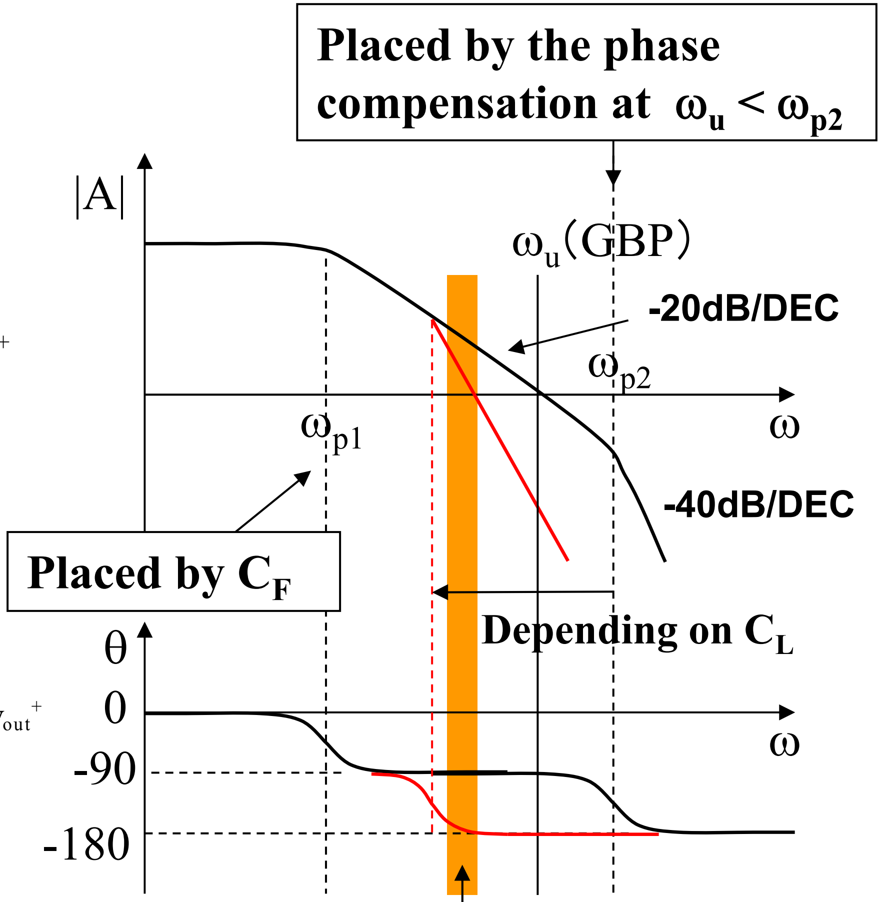
Class AB output buffer
（See chapter 14)

The output buffer may be omitted to reduce the power consumption, if the OPA drive only the capacitive load or operate with high loop gain.

AC characteristic of OPA



$$V_{out}^{+} = \frac{1}{1+j\omega\cdot R_{out3}C_L}V_2 = \frac{1}{1+j\omega/\omega_{p2}}V_2$$



Placed by the phase compensation at $\omega_u < \omega_{p2}$

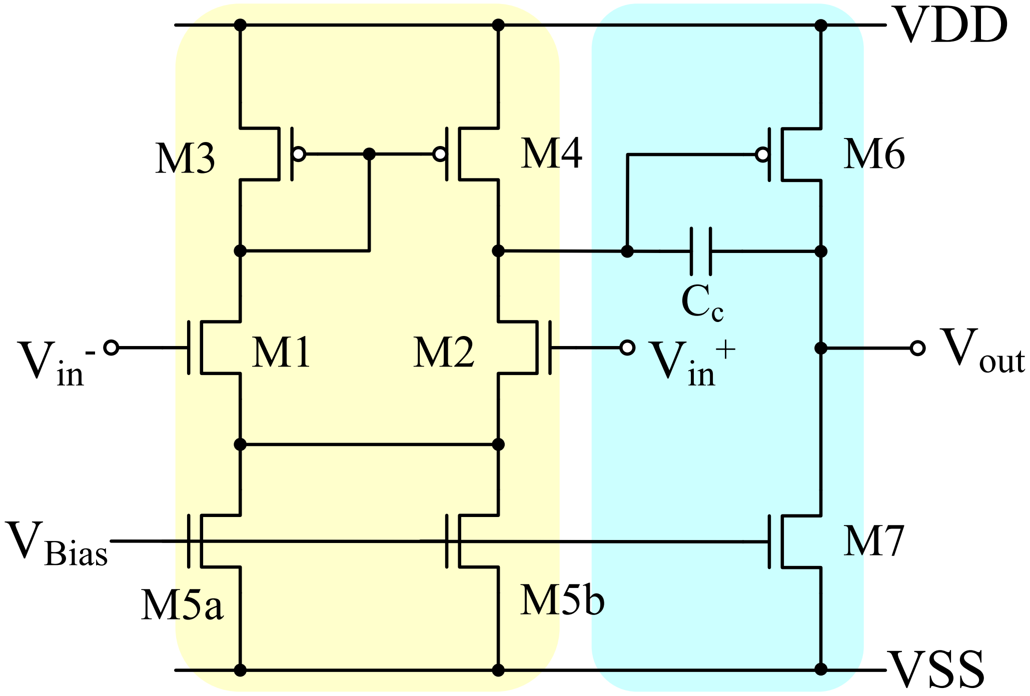
Placed by C_F

Depending on C_L

The phase margin is decreased for the very large C_L.

12.2 Analysis of 2-stage CS OPA

Structure of 2-stage OPA



Differential amplifier CS amplifier

$$A_d = g_{m1} \cdot (r_{ds2} // r_{ds4}) \cdot g_{m6} \cdot (r_{ds6} // r_{ds7})$$

(without the output buffer)

Bias current dependence of the differential gain

Differential amplifier stage

$$A_{V1} = -g_{m1} \cdot (r_{ds2} // r_{ds4})$$

$$g_{m1} = \sqrt{2\beta_1 I_{DS1}}$$

$$r_{ds2} = \frac{1}{\lambda_2 I_{DS2}} = \frac{1}{\lambda_2 I_{DS1}}$$

$$r_{ds4} = \frac{1}{\lambda_4 I_{DS4}} = \frac{1}{\lambda_4 I_{DS1}}$$

CS amplifier stage

$$A_{V2} = -g_{m6} \cdot (r_{ds6} // r_{ds7})$$

$$g_{m6} = \sqrt{2\beta_6 I_{DS6}}$$

$$r_{ds6} = \frac{1}{\lambda_6 I_{DS6}} = \frac{1}{\lambda_6 I_{DS6}}$$

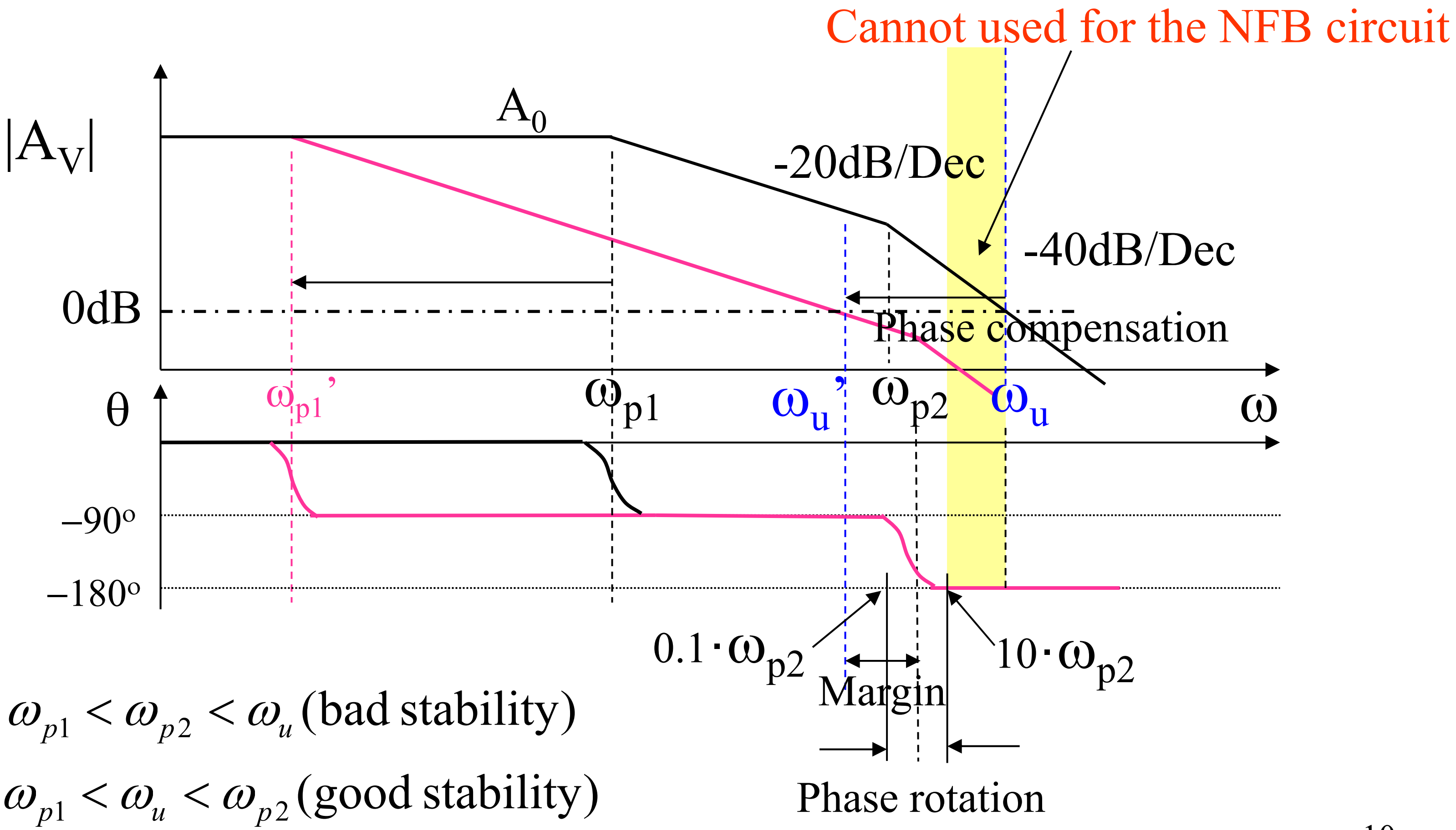
$$r_{ds7} = \frac{1}{\lambda_7 I_{DS7}} = \frac{1}{\lambda_7 I_{DS6}}$$

Total gain

$$A_d = A_{V1} A_{V2} = \frac{g_{m1} g_{m6}}{(g_{ds2} + g_{ds4})(g_{ds6} + g_{ds7})} = \frac{2\sqrt{\beta_1 \beta_6}}{(\lambda_2 + \lambda_4)(\lambda_6 + \lambda_7)} \frac{1}{\sqrt{I_{DS1} I_{DS6}}}$$

Phase compensation (1)

Constraint for ω_{p2} and ω_u



$\omega_{p1} < \omega_{p2} < \omega_u$ (bad stability)

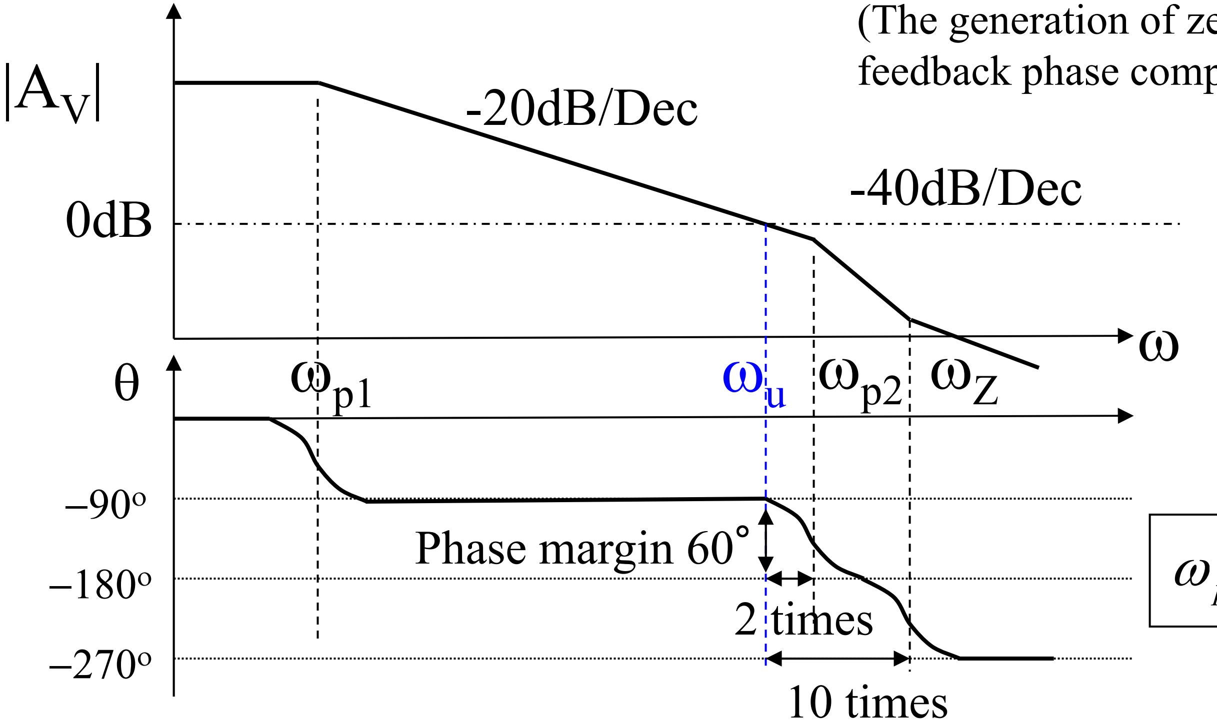
$\omega_{p1} < \omega_u < \omega_{p2}$ (good stability)

Phase compensation (2)

Constraint for ω_z and ω_u

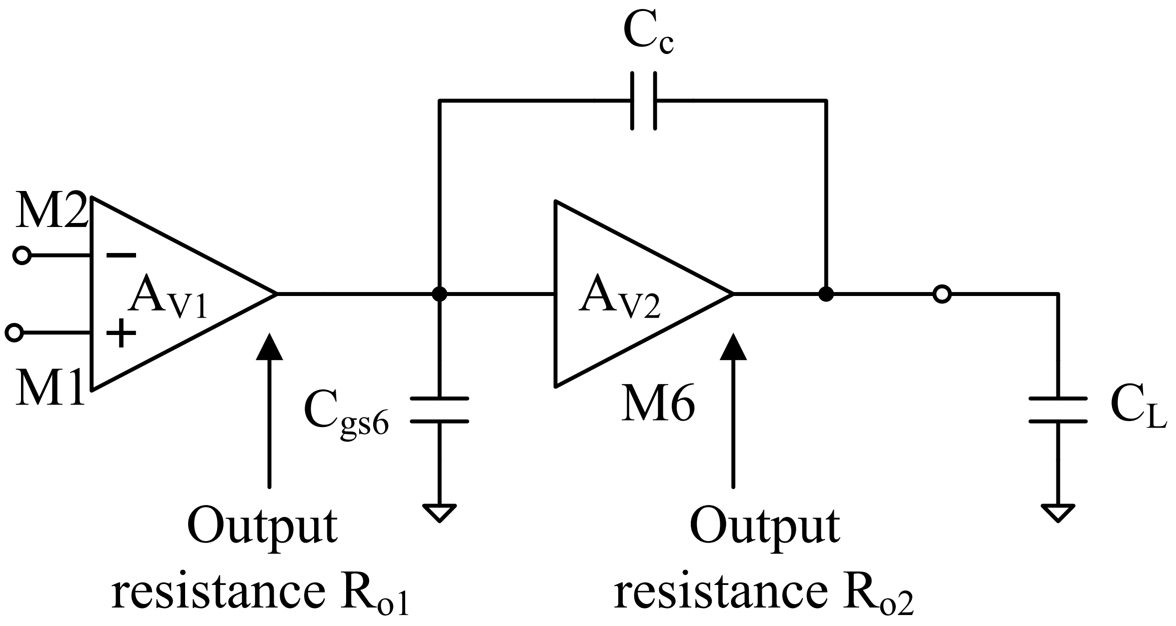
Constraint for ω_{p2} and ω_z $\begin{cases} \omega_{p2} \geq 2 \cdot \omega_u \\ \omega_z \geq 10 \cdot \omega_u \end{cases}$

(The generation of zero is inevitable in the feedback phase compensation circuit.)



$$\boxed{\omega_{p1} < \omega_u < \omega_{p2} < \omega_z}$$

Miller capacitance phase compensation technique



The input parasitic capacitance of M6 is C_{gs6}, but the input capacitance of the 2nd amplifier is controlled by the Miller capacitance C_M.

$$C_M = A_{V2} \cdot C_C + C_{gs6} \approx A_{V2} \cdot C_C$$

Design of the frequency response

Pole and Zero frequency and the circuit parameters

$$\omega_{p1} \cong \frac{1}{(A_{V2}C_C)\cdot R_{o1}}$$ (Miller effect)

$$\omega_u \cong A_{V1}\cdot A_{V2}\cdot\omega_{p1} = \frac{A_{V1}}{C_C\cdot R_{o1}} = \frac{g_{m1}}{C_C}$$ (Miller effect)

$$\omega_Z \cong \frac{g_{m6}}{C_C}$$ (Feed forward through C_c)

$$\omega_{p2} \cong \frac{1}{C_L\cdot R_{o2}} \cong \frac{g_{m6}}{C_L}$$ (The output capacitance of 2nd amplifier)

↑

In the frequency range more than ω_u, the input signal and output signal level is comparable, approximately, $A_{V2}=G_{m2}\cdot R_{o2}= -g_{m6}\cdot R_{o2} \fallingdotseq -1$.

Constraint of the phase compensation

60° Phase margin

$$\boxed{\omega_{p2} > 2\omega_u}$$

$$\frac{g_{m6}}{C_L} > 2\frac{g_{m1}}{C_C}$$

Separation between ω_z and ω_u

$$\boxed{\omega_Z > 10\omega_u}$$

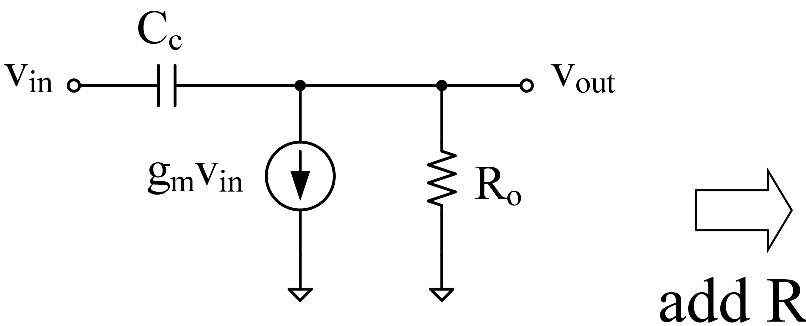
$$\frac{g_{m6}}{C_C} > 10\frac{g_{m1}}{C_C}$$

Phase compensation Constraint

$$\left\{\begin{array}{l} g_{m6} \geq 10 g_{m1} \\ C_C \geq 0.2 C_L \end{array}\right.$$

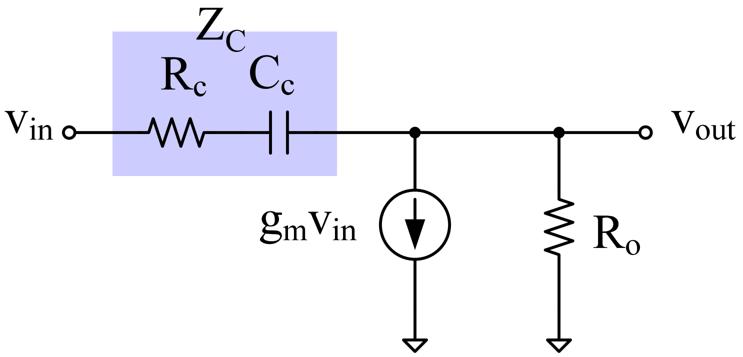
Location of the zero (1)

The phase compensation using C_C requires the constraint $g_{m6} > 10g_{m1}$ to remove the influence of ω_Z. this method requires the very large g_{m6}. RC phase compensation can be used to evade this problem.



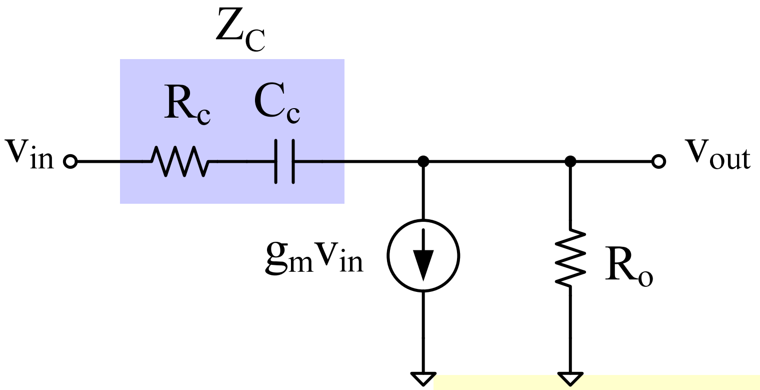
add R_c

$$\frac{v_{out}}{v_{in}} = \frac{R_O g_m (1 - j\omega \cdot C_C \frac{1}{g_m})}{1 + j\omega \cdot C_C R_O}$$



$$\frac{v_{out}}{v_{in}} = \frac{R_O g_m (1 - \frac{1}{Z_C g_m})}{1 + \frac{R_O}{Z_C}}$$

Location of the zero (2)



$$\omega_Z = \frac{1}{C_C\left(\frac{1}{g_m} - R_C\right)}$$

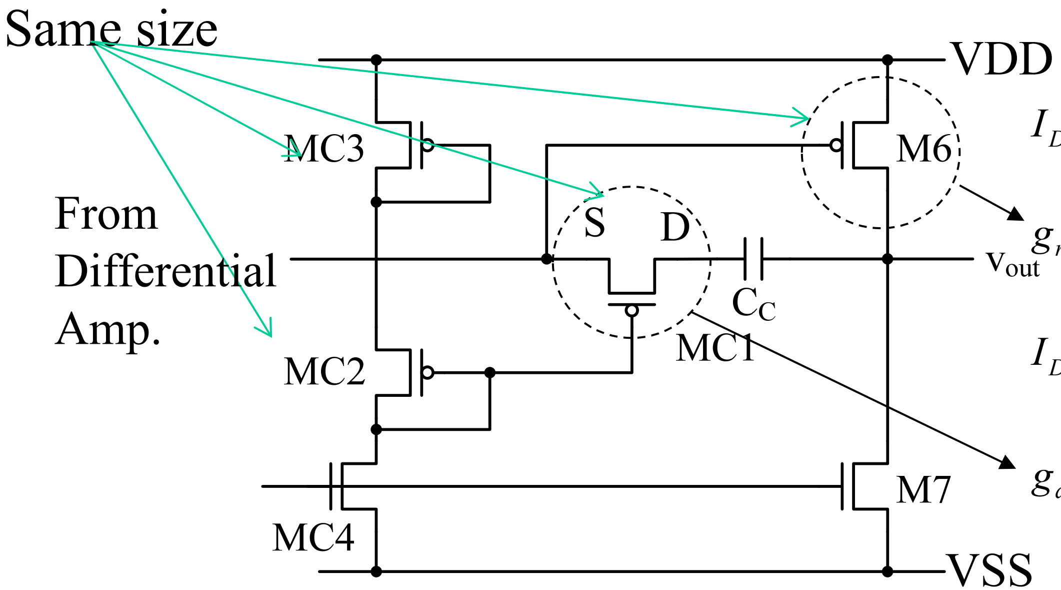
$$\frac{v_{out}}{v_{in}} = \frac{-R_O g_m \left(1 - \frac{1}{Z_C g_m}\right)}{1 + \frac{R_O}{Z_C}}$$

$$= \frac{-R_O g_m \{1 - j\omega \cdot C_C(\frac{1}{g_m} - R_C)\}}{1 + j\omega \cdot C_C(R_O + R_C)}$$

$$= \frac{-R_O g_m \{1 - j\omega / \omega_Z\}}{1 + j\omega / \omega_{p3}}$$

Method (1) : If $R_C = 1/g_m$, $\omega_Z \to \infty$ (Nulling the zero)
Method (2) : If $R_C > 1/g_m$, ω_Z is located in the left half plane (the phase turns counterclockwise.)

Practical R_c implementation by MOSFET output conductance



$$I_{DS6} = \frac{\beta_p}{2}(V_{GS6} - V_{Tp})^2$$

$$g_{m6} = \frac{\partial I_{DS6}}{\partial V_{GS6}} = \beta_p(V_{GS6} - V_{Tp})$$

$$I_{DS\_MC1} = \beta_p\{(V_{GS\_MC1} - V_{Tp})V_{DS\_MC1} - \frac{1}{2}V^2_{DS\_MC1}\}$$

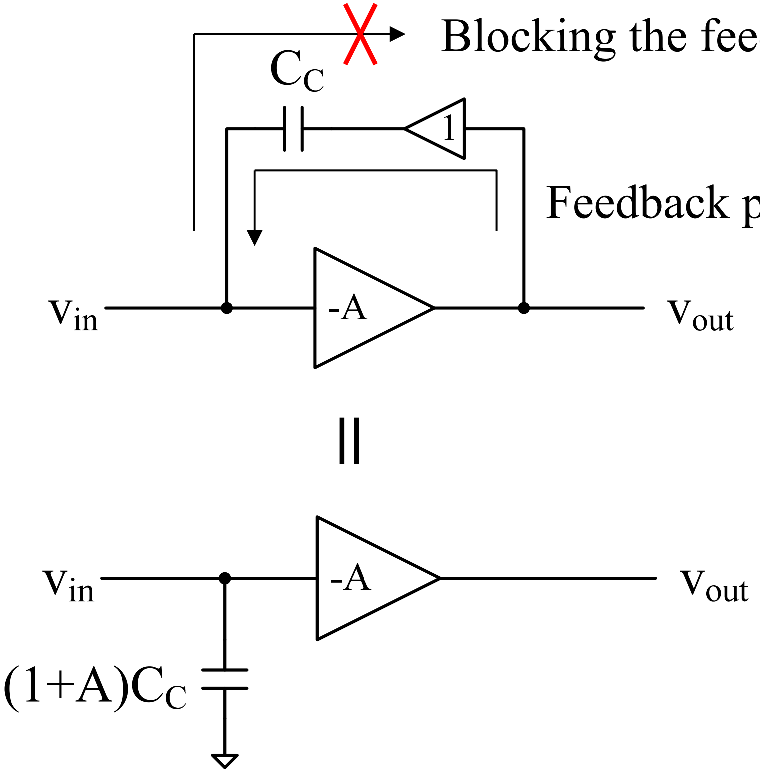
$$g_{ds\_MC1} = \left.\frac{\partial I_{DS\_MC1}}{\partial V_{DS\_MC1}}\right|_{V_{DS\_MC1}=0} = \beta_p(V_{GS\_MC1} - V_{Tp})$$

M7 and MC4 are the same size.
M6, MC1, MC2, and MC3 are the same size.

$g_{m6} = g_{ds\_MC1}$, $\omega_z \rightarrow \infty$
(see slide 16)

$$V_{GS\_MC3} + V_{GS\_MC2} = V_{GS6} + V_{GS\_MC1}$$
$$V_{GS\_MC1} = V_{GS\_MC3} + V_{GS\_MC2} - V_{GS6} = V_{GS6} + V_{GS6} - V_{GS6} = V_{GS6}$$

Indirect phase compensation (1)



Blocking the feedforward path by the feedback buffer amplifier

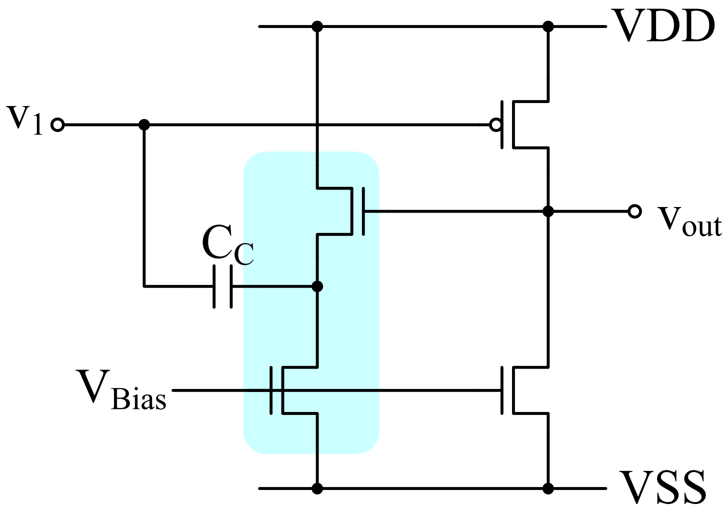
Feedback path

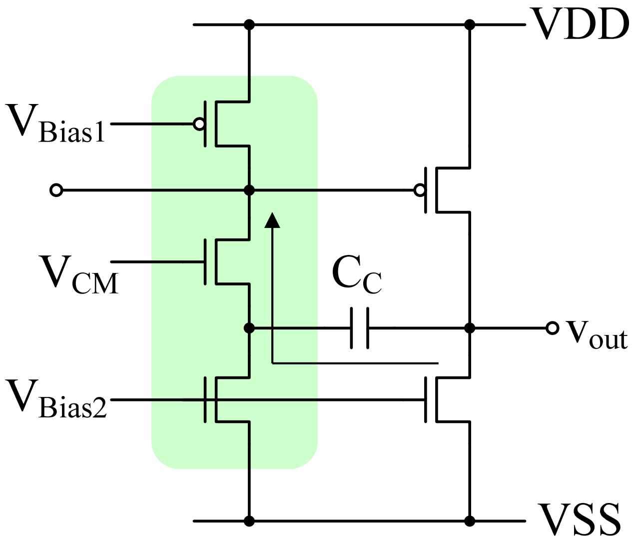
$$i_{in} = j\omega \cdot C(v_{in} - v_{out})$$

$$v_{out} = -A \cdot v_{in}$$

$$\frac{i_{in}}{v_{out}} = j\omega \cdot C(1 + A)$$

Indirect phase compensation (2)


Source follower feedback buffer


Common-gate feedback buffer

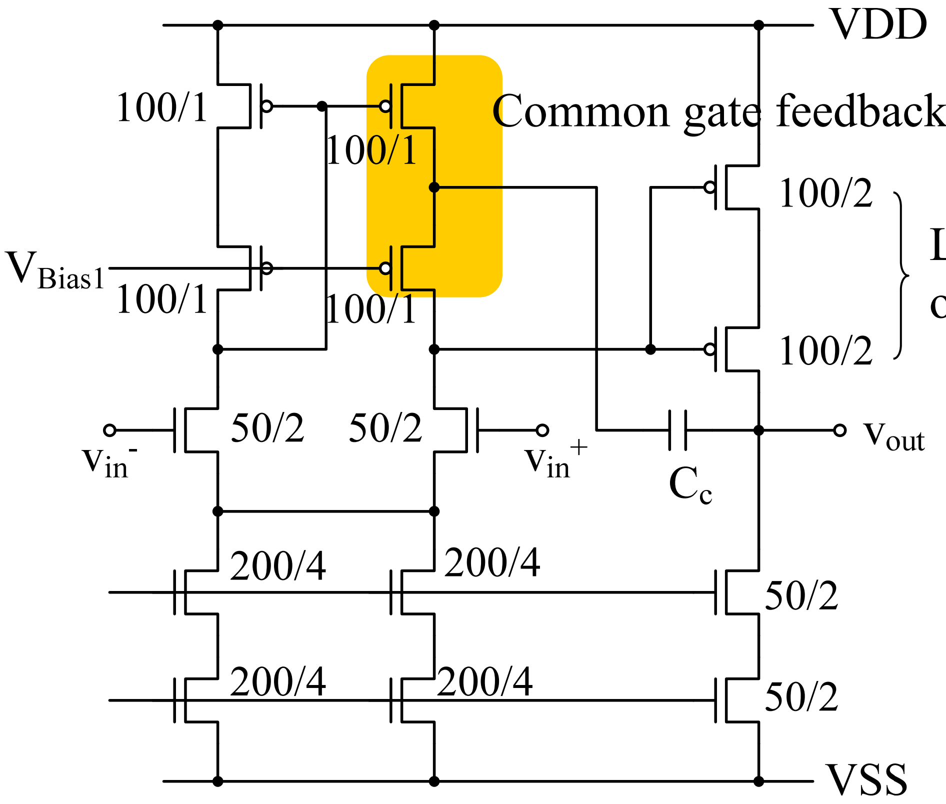
Advantages:

- High SR, High ω_{p2}, High ω_u, small C_c

Disadvantage:

- Additional power consumption

Indirect phase compensation (3)



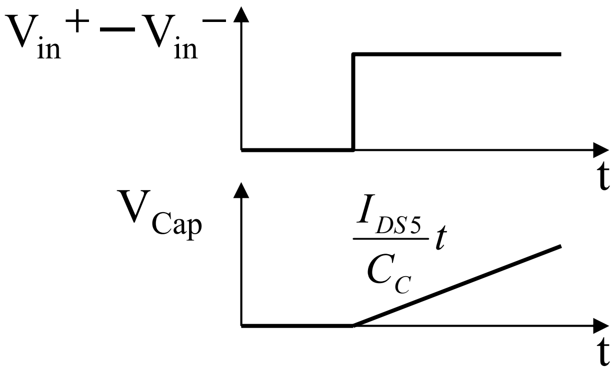
Common gate feedback buffer

Long L will help the adjustment of the output offset voltage.

The cascode current mirror load is used in place of the feedback buffer. There is no additional power consumption.

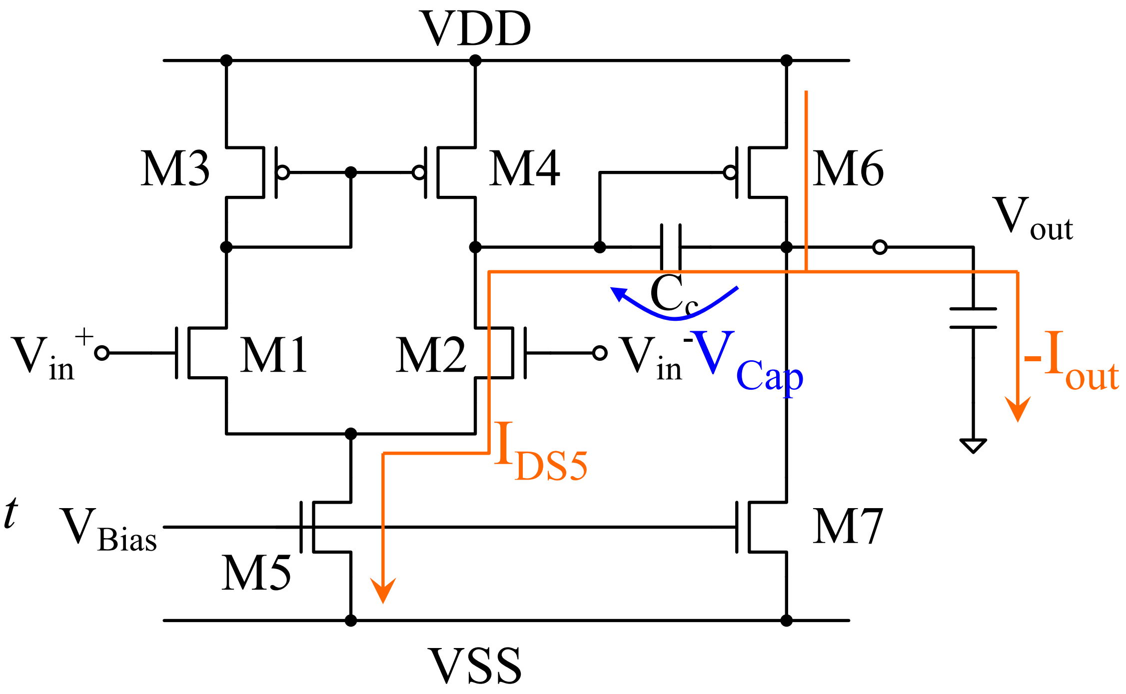
12.3 Optimization of MOSFET size

I_{SS} and SR



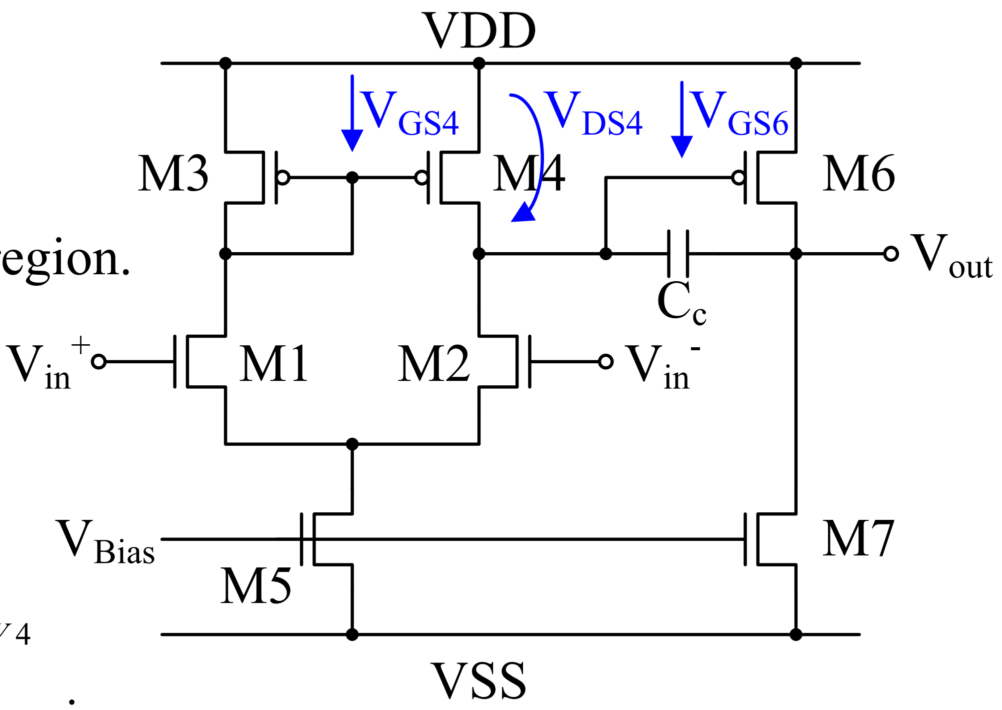
$$V_{Cap} = \frac{1}{C_C}\int I_{DS5}\,dt = \frac{I_{DS5}}{C_C}\cdot t$$

$$\boxed{SR = \frac{I_{DS5}}{C_C}}$$



SR is limited by the current I_{SS} (I_{DS5}) and I_{out}.

Saturation of M4 (1)



$$V_{DS3} \geq V_{GS3} - V_{Tp} = \Delta_{OV3}$$

M3 always operates in the saturation region.

$$V_{DS4} = V_{GS6}$$

If $V_{GS4} = V_{GS6}$,

$$V_{DS4} = V_{GS6} = V_{GS4} \geq V_{GS4} - V_{Tp} = \Delta_{OV4}$$

M4 always operates in the saturation region.

⇩

MOSFET size should be optimized for $V_{GS4} = V_{GS6}$.

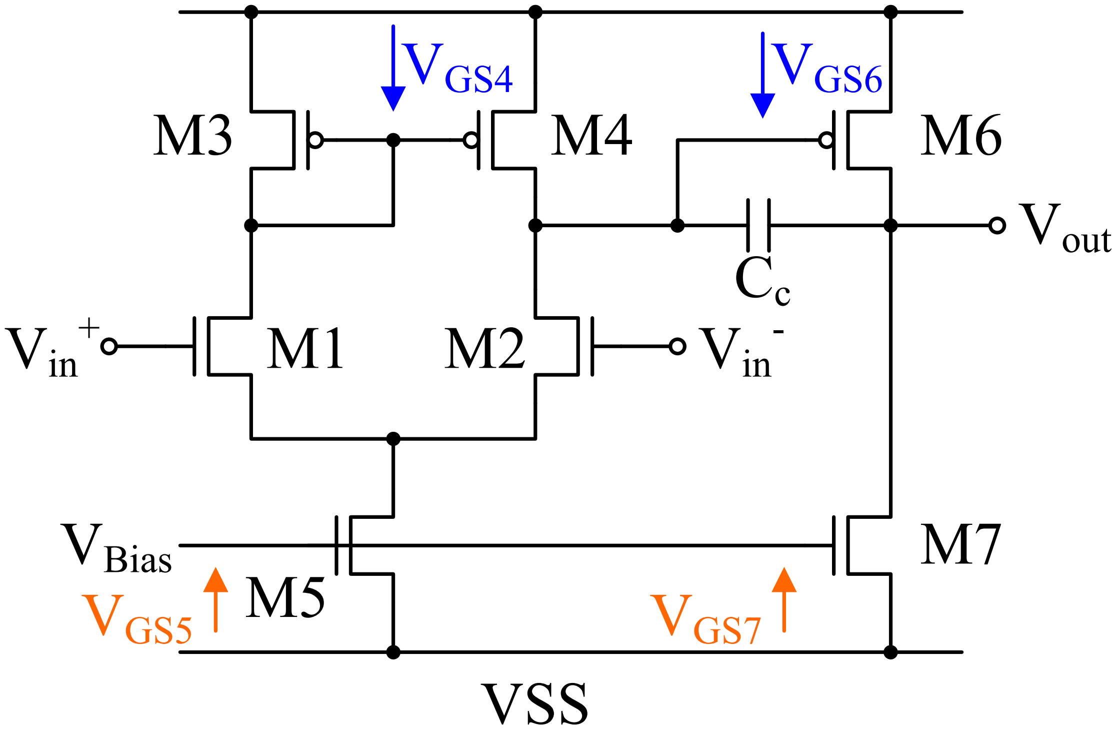
Saturation of M4 (2)

If $V_{GS4} = V_{GS6}$,

$$\frac{I_{DS6}}{I_{DS4}} = \frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_4}$$

$$V_{GS5} = V_{GS7}$$

$$\frac{I_{DS7}}{I_{DS5}} = \frac{\left(\frac{W}{L}\right)_7}{\left(\frac{W}{L}\right)_5}$$



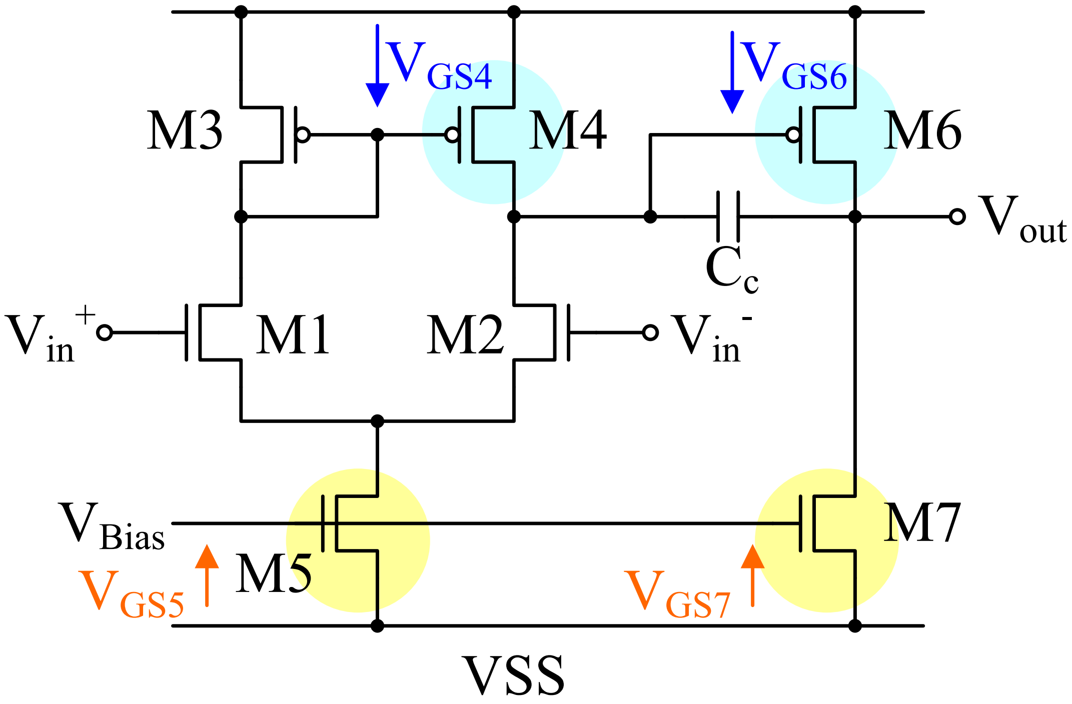
Saturation of M4 (3)

$$\begin{cases} I_{DS6} = I_{DS7} \\ I_{DS5} = 2I_{DS4} \end{cases}$$

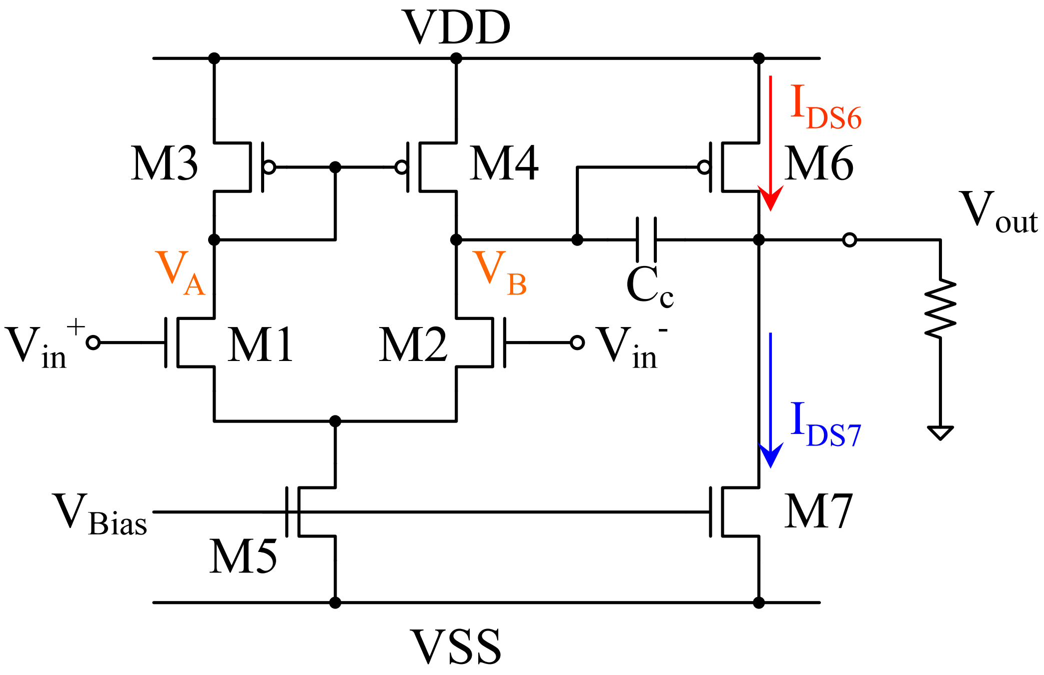
$$\frac{I_{DS6}}{I_{DS4}} = 2\frac{I_{DS7}}{I_{DS5}}$$

Saturation condition of M4

$$\frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_4} = 2\frac{\left(\frac{W}{L}\right)_7}{\left(\frac{W}{L}\right)_5}$$



Systematic offset (1)



Systematic offset

  Current balance of M6 and M7

Random offset

  Process variation of V_T

When $V_A = V_B$ (differential input = 0),
the output current = 0 or $I_{DS6} = I_{DS7}$.

Systematic offset (2)

$$\left.\begin{array}{l}\begin{cases} I_{DS3} = \dfrac{\beta_3}{2}(V_A - V_{Tp})^2 \\ I_{DS5} = \dfrac{\beta_5}{2}(V_{Bias} - V_{Tn})^2 \\ I_{DS6} = \dfrac{\beta_6}{2}(V_B - V_{Tp})^2 \\ I_{DS7} = \dfrac{\beta_7}{2}(V_{Bias} - V_{Tn})^2 \end{cases} \\ \text{When } V_A = V_B, \\ \begin{cases} I_{DS6} = I_{DS7} \longleftarrow \text{slide 26} \\ I_{DS3} = \dfrac{I_{DS5}}{2} \end{cases}\end{array}\right\} \Rightarrow$$

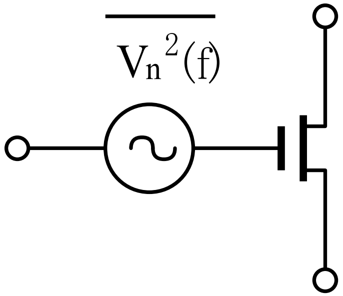
This constraint is same as the saturation constraint of M4.

$$\frac{\beta_6}{\beta_3} = 2\frac{\beta_7}{\beta_5}$$

$$\frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_4} = 2\frac{\left(\frac{W}{L}\right)_7}{\left(\frac{W}{L}\right)_5}$$

Input-referred noise (1)

Channel noise model of MOSFET



Thermal noise Flicker noise

$$\overline{V_n^2(f)} = 4kT\gamma \frac{g_{ds}}{g_m^2} + \frac{K_{p/n}}{WLC_{OX}^2}\frac{1}{f} \qquad (V^2/Hz)$$

$$\gamma = \begin{cases} 2/3 & \text{(Long Channel)} \\ 1 & \text{(Short Channel)} \end{cases} \qquad \begin{cases} K_p \cong 10^{-24} & (V^2/F) \\ K_n \cong 10^{-23} & (V^2/F) \end{cases}$$

The channel noise is observed in the output terminal, but the noise PSD is normally described as a input-referred noise PSD.

NOTE: Large L is better for the low noise amplifier, because of large L*W.

Input-referred noise (2)

Intrinsic noise density of the differential amplifier

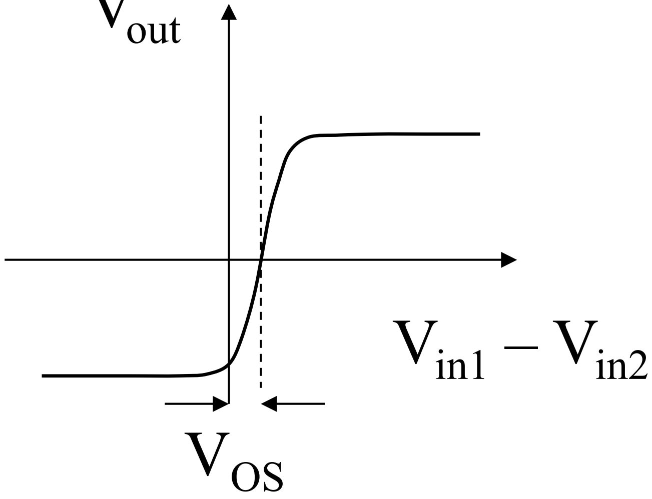
Thermal noise $$\overline{V_n^2(f)} = 4kT\left(\frac{1}{g_{m1}} + \frac{g_{m3}}{g_{m1}^2}\right)$$ (Total noise from M1 and M3)

Flicker noise $$\overline{V_n^2(f)} = \frac{K_n}{W_1 L_1 C_{OX}{}^2}\left(1 + \frac{K_p}{K_n}\frac{W_1 L_1}{W_3 L_3}\right)\frac{1}{f}$$

NOTE: Assuming that the differential pair consists n-ch MOFET
and current mirror load consists p-ch MOSFETs.

Mismatch of MOSFETs by the process variation

$$\begin{aligned}
V_{OS\_1-2} &= V_{GS1} - V_{GS2} \\
&= V_{Tn1} + \sqrt{\frac{I_{DS5}}{\beta_1}} - V_{Tn2} - \sqrt{\frac{I_{DS5}}{\beta_2}} \\
&= (V_{Tn1} - V_{Tn2}) + \sqrt{\frac{I_{DS5}}{\beta_1}}[1 - \sqrt{\frac{\beta_1}{\beta_2}}] \\
&\cong (V_{Tn1} - V_{Tn2}) - \frac{1}{2}\sqrt{\frac{I_{DS5}}{\beta_1}}[\frac{\beta_1 - \beta_2}{\beta_1}] \\
&= \Delta V_{Tn1-2} - \frac{V_{GS1} - V_{Tn1}}{2}[\frac{\Delta\beta}{\beta_1}]_{1-2} = \Delta V_{Tn1-2} - \frac{\Delta_{OV1}}{2}[\frac{\Delta\beta}{\beta_1}]_{1-2}
\end{aligned}$$



$$\begin{aligned}
V_{OS\_3-4} &= V_{GS3} - V_{GS4} \\
&\cong \Delta V_{Tn3-4} - \frac{V_{GS3} - V_{Tp3}}{2}[\frac{\Delta\beta}{\beta_3}]_{3-4} = \Delta V_{Tn3-4} - \frac{\Delta_{OV3}}{2}[\frac{\Delta\beta}{\beta_3}]_{3-4}
\end{aligned}$$

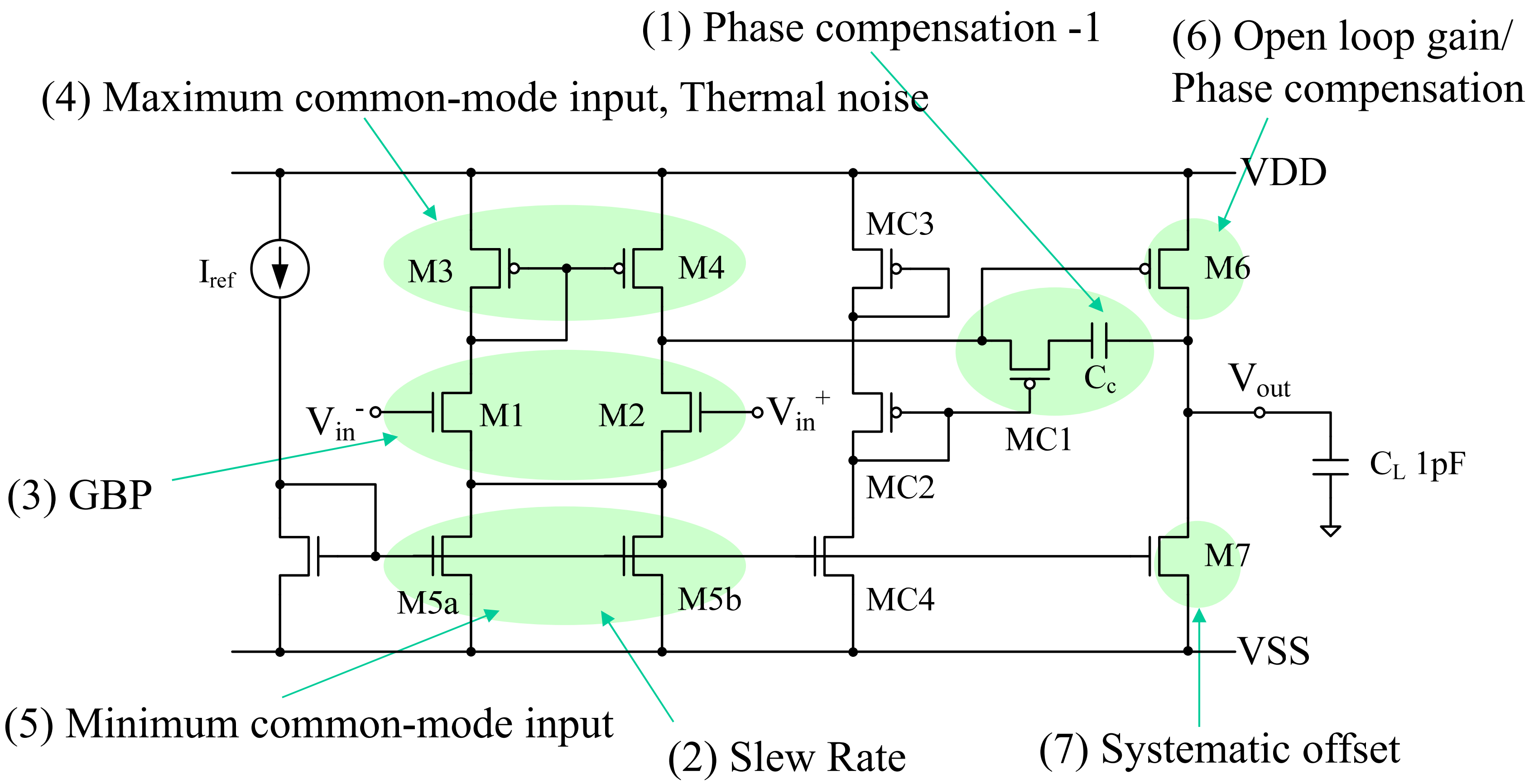
$$V_{OS} = \Delta V_{Tn1-2} - \frac{\Delta_{OV1}}{2}[\frac{\Delta\beta}{\beta_1}]_{1-2} + \frac{g_{m3}}{g_{m1}}[\Delta V_{Tn3-4} - \frac{\Delta_{OV3}}{2}[\frac{\Delta\beta}{\beta_3}]_{3-4}]$$

Optimization for the noise and process variation

- Thermal noise
  - Differential pair MOSFETs: Large W/L
  - Current mirror load MOSFETs: Small W/L
- Flicker noise
  - Differential pair MOSFETs: Large W*L
  - Current mirror load MOSFETs: Large W*L
- Mismatch offset
  - Differential pair MOSFETs: Large W, L
  - Current mirror load MOSFETs: Small W/L (Small g_{m3}/g_{m1})

NOTE: Consider that the L and W influences the frequency response too.

Design constraints



(1) Phase compensation -1

(6) Open loop gain/
Phase compensation

(4) Maximum common-mode input, Thermal noise

(3) GBP

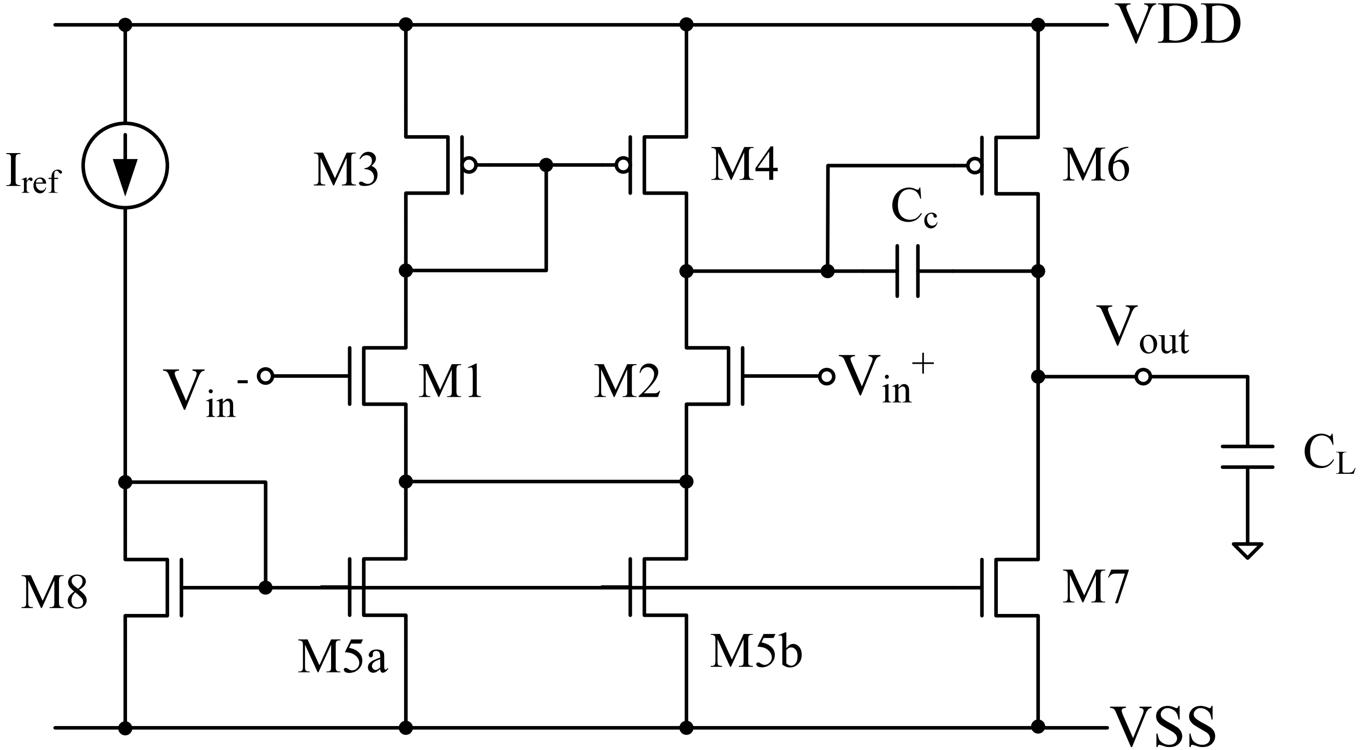
(5) Minimum common-mode input

(2) Slew Rate

(7) Systematic offset

12.4 Design example of a single-end OPA

Circuit topology



2 stage OPA without zero-canceling

Specification

Power supply voltage	VDD/VSS	2.5V/-2.5V
Open loop gain	Ad	> 95dB
GBP	f_u	100MHz
Phase margin	PM	60°
Slew rate	SR	> 100 V/us
Load capacitance	C_L	1.0 pF
Output voltage swing	$Vout_{p\text{-}p}$	> 4.2 V
Maximum common-mode voltage	Vin^{max}	> 2.1 V
Minimum common-mode voltage	Vin^{min}	< -1.4 V
Input-referred noise	$\sqrt{v_n^2}$	< 500 uV (BW=1Hz~1MHz)
Power consumption	PW	< 10 mW

Parameters of MOSFET

Parameter		n-ch	p-ch
V_T	[V]	0.78	-0.86
μC_{OX}	[A/V^2]	98u	33u
λ	[1/V]	0.0186	0.0114

The parameters are extracted from 10um/2um MOSFETs for Δ_{OV} =0.2V.

Cc, I_{SS}

(1) Phase compensation -1

$$\begin{cases} \text{Load capacitance} & C_L = 1.0\ \text{pF} \\ \text{Phase compensation constraint} & C_C \geq 0.2 C_L \end{cases}$$

$$C_C = 0.2\ \text{pF}$$

(2) SR

$$SR = \frac{I_{DS5}}{C_C}$$

$$I_{DS5} = SR \cdot C_C = 100\text{MV/s} \cdot 0.2\text{pF} = 20\text{uA}$$

$$I_{DS3} = I_{DS4} = I_{DS1} = I_{DS2} = \frac{I_{DS5}}{2} = 10\text{uA}$$

M1, M2

(3) GBP

$$\omega_u = \frac{g_{m1}}{C_C}$$

$$g_{m1} = C_C \omega_u = 0.2\text{p} \cdot 2\pi \cdot 100\text{M} = 126\text{uS}$$

(2) I_{DS1} & (3) g_{m1}

$$g_{m1} = \sqrt{2\beta_1 I_{DS1}} = \sqrt{2\mu_n C_{OX} \left(\frac{W}{L}\right)_1 I_{DS1}} = 126\text{uS}$$

$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \frac{g_{m1}^2}{2\mu_n C_{OX} I_{DS1}} = \frac{(126\text{u})^2}{2 \cdot 98\text{u} \cdot 10\text{u}} = 8.1 \approx 10$$

$$\Delta_{OV} = \sqrt{\frac{2I_{DS1}}{\beta_1}} = \sqrt{\frac{2 \cdot 10\text{u}}{98\text{u} \cdot 10}} = 0.143\text{V}$$

M3, M4

(4) Maximum common-mode input

$$\begin{cases} V_{in}^{\max} = VDD - \Delta_{OV3} - \left|V_{Tp}\right| + V_{Tn} \\ \Delta_{OV3} = \sqrt{\dfrac{2I_{DS3}}{\beta_3}} = VDD - \left|V_{Tp}\right| + V_{Tn} - V_{in}^{\max} \end{cases}$$

$$\beta_3 = \frac{2I_{DS3}}{(VDD - \left|V_{Tp}\right| + V_{Tn} - V_{in}^{\max})^2}$$

$$\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = \frac{2I_{DS3}}{\mu_p C_{OX}} \frac{1}{(VDD - \left|V_{Tp}\right| + V_{Tn} - V_{in}^{\max})^2}$$

$$= \frac{2 \cdot 10\text{u}}{33\text{u}} \frac{1}{(2.5 - 0.86 + 0.78 - 2.1)^2} = 5.9 \approx 6$$

M5

(5) Minimum common-mode input

$$\begin{cases} V_{in}^{\min} = VSS + V_{Tn} + \Delta_{OV1} + \Delta_{OV5} \\ \Delta_{OV5} = \sqrt{\dfrac{2I_{DS5}}{\beta_5}} = V_{in}^{\min} - \Delta_{OV1} - V_{Tn} - VSS \end{cases}$$

$$\Delta_{OV1} = \sqrt{\frac{2I_{DS1}}{\beta_1}} = \sqrt{\frac{2\cdot 10\text{u}}{98\text{u}\cdot 10}} = 0.143\text{V}$$

$$\beta_5 = \frac{2I_{DS5}}{(V_{in}^{\min} - \Delta_{OV1} - V_{Tn} - VSS)^2}$$

$$\left(\frac{W}{L}\right)_5 = \frac{2I_{DS5}}{\mu_n C_{OX}} \frac{1}{(V_{in}^{\min} - \Delta_{OV1} - V_{Tn} - VSS)^2}$$

$$= \frac{2\cdot 10\text{u}}{98\text{u}} \frac{1}{(-1.4 - 0.143 - 0.78 + 2.5)^2} = 6.51 \approx 8$$

M6 (without zero cancellation)

(6) Phase compensation -2

$$\begin{aligned} g_{m6} &\geq 10 g_{m1} \\ &= 10 \cdot \sqrt{2\beta_1 I_{DS1}} \\ &= 10 \cdot \sqrt{2 \cdot 98\text{u} \cdot 10 \cdot 10\text{u}} \\ &= 1.40\text{mS} \end{aligned}$$

If $V_{GS4} = V_{GS6}$,

$$\left\{ \begin{aligned} \frac{I_{DS6}}{I_{DS4}} &= \frac{\beta_6}{\beta_4} \\ g_{m6} &= \sqrt{2\beta_6 I_{DS6}} \end{aligned} \right.$$

$$\beta_6 = g_{m6} \sqrt{\frac{\beta_4}{2 I_{DS4}}}$$

$$\begin{aligned} \left(\frac{W}{L}\right)_6 &= \frac{g_{m6}}{\mu_p C_{OX}} \sqrt{\frac{\beta_4}{2 I_{DS4}}} \\ &= \frac{1.40\text{m}}{33 \cdot 10^{-6}} \sqrt{\frac{33\text{u} \cdot 6}{2 \cdot 10\text{u}}} \\ &= 133.48 \approx 138 \end{aligned}$$

Bias condition:

$$I_{DS6} = \frac{\beta_6}{\beta_4} I_{DS4} = \frac{138}{6} 10\text{u} = 230\text{uA}$$

$$\Delta_{OV6} = \sqrt{\frac{2 I_{DS6}}{\beta_6}} = \sqrt{\frac{2 \cdot 230\text{u}}{33\text{u} \cdot 138}} = 0.318\text{V}$$

M7

(7) Systematic offset (Saturation of M4)

$$\left(\frac{W}{L}\right)_7 = \frac{1}{2}\left(\frac{W}{L}\right)_5 \frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_4}$$

$$= \frac{1}{2} 8 \frac{138}{6} = 92$$

The circuit parameters are determined. Check the other specification.

Output swing

$$V_{out}^{\min} = VSS + \Delta_{OV7} = VSS + \sqrt{\frac{2I_{DS7}}{\mu_n C_{OX}\left(\frac{W}{L}\right)_7}}$$

$$= -2.5 + \sqrt{\frac{2 \cdot 230\text{u}}{98\text{u} \cdot 92}}$$

$$\approx -2.27\text{V}$$

$$V_{out}^{\max} = VDD - \Delta_{OV6}$$

$$= VDD - \sqrt{\frac{2I_{DS6}}{\mu_p C_{OX}\left(\frac{W}{L}\right)_6}}$$

$$= 2.5 - \sqrt{\frac{2 \cdot 230\text{u}}{33\text{u} \cdot 138}}$$

$$\approx 2.18 \quad \text{V}$$

Output voltage swing $V_{\text{out, p-p}}$ = 4.45 V

Open loop gain

$$
\begin{aligned}
A_d &= A_{V1} \cdot A_{V2} \\
&= g_{m1}(r_{ds2} // r_{ds4}) \cdot g_{m6}(r_{ds6} // r_{ds7}) \\
&= \frac{\sqrt{2\beta_1 I_{DS1}}}{I_{DS1}(\lambda_n + \lambda_p)} \cdot \frac{\sqrt{2\beta_6 I_{DS6}}}{I_{D6}(\lambda_n + \lambda_p)} \\
&= \frac{\sqrt{\frac{2 \cdot 98\mathrm{u} \cdot 10}{10\mathrm{u}}}}{(0.0186 + 0.114)} \frac{\sqrt{\frac{2 \cdot 33\mathrm{u} \cdot 138}{230\mathrm{u}}}}{(0.0186 + 0.0114)} \\
&= 466 \cdot 210 \\
&= 97749 = 99.8\mathrm{dB}
\end{aligned}
$$

Flicker noise (1)

$$V_{nf}^2 = \frac{K_n}{W_1 L_1 C_{OX}{}^2}\{1+\frac{K_p}{K_n}\frac{W_1 L_1}{W_3 L_3}\}\frac{1}{f} \quad (\mathrm{V}^2/\mathrm{Hz})$$

$$NL_f^2 = \int_{f_l}^{f_u} V_{nf}^2 df = \frac{K_n}{W_1 L_1 C_{OX}{}^2}(1+\frac{K_p}{K_n}\frac{W_1 L_1}{W_3 L_3})\ln(f_u / f_l) \quad (\text{frequency range} \quad f_u \sim f_u)$$

$$= \frac{K_n}{W_1 L_1 C_{OX}{}^2}(1+\frac{K_p}{K_n}\frac{W_1}{W_3})\ln(f_u / f_l) \quad (\text{for } L_1 = L_3)$$

$$C_{OX} = \frac{\varepsilon_0 \varepsilon_{Si}}{t_{OX}} = 2.5 \cdot 10^{-3}\,\mathrm{F/m^2}$$

The parameter C_{OX} can be loosely estimated for $\mu_n C_{OX}$ or $\mu_p C_{OX}$. Say $\mu_n \sim$ 400 cm^2/Vs and $\mu_p \sim$ 130 cm^2/Vs.

Flicker noise (2)

Based on the specification sheet, at f_u = 1 MHz, V_{nf} = 500 μV.

$$(500\text{uV})^2 \ge NL_f^2$$

$$2.5 \cdot 10^{-7} \ge \frac{10^{-24}}{W_1 L_1 \cdot (2.5 \cdot 10^{-3})^2}(1 + 0.1\frac{10}{6})\ln(1 \cdot 10^6 / 1 \cdot 10^{-1}) \quad \text{V}^2$$

$$= \frac{3.009 \cdot 10^{-18}}{W_1 L_1}$$

$$\begin{cases} W_1 L_1 \ge 1.203 \cdot 10^{-11} \quad \text{m}^2 \\ \dfrac{W_1}{L_1} = 10 \end{cases}$$

$$\therefore L_1 \ge 1.096\text{um} \quad \longrightarrow \quad L_1 \approx 2\text{um}$$

Thermal noise

$$V_{nt}^2 = \frac{8}{3} kT\left(\frac{1}{g_{m1}} + \frac{g_{m3}}{g_{m1}^2}\right) \qquad \mathrm{V^2/Hz}$$

$$NL_t^2 = \frac{8}{3} kT\left(\frac{1}{g_{m1}} + \frac{g_{m3}}{g_{m1}^2}\right)\Delta f \quad \text{(frequency range } 0 \sim f_u\text{)}$$

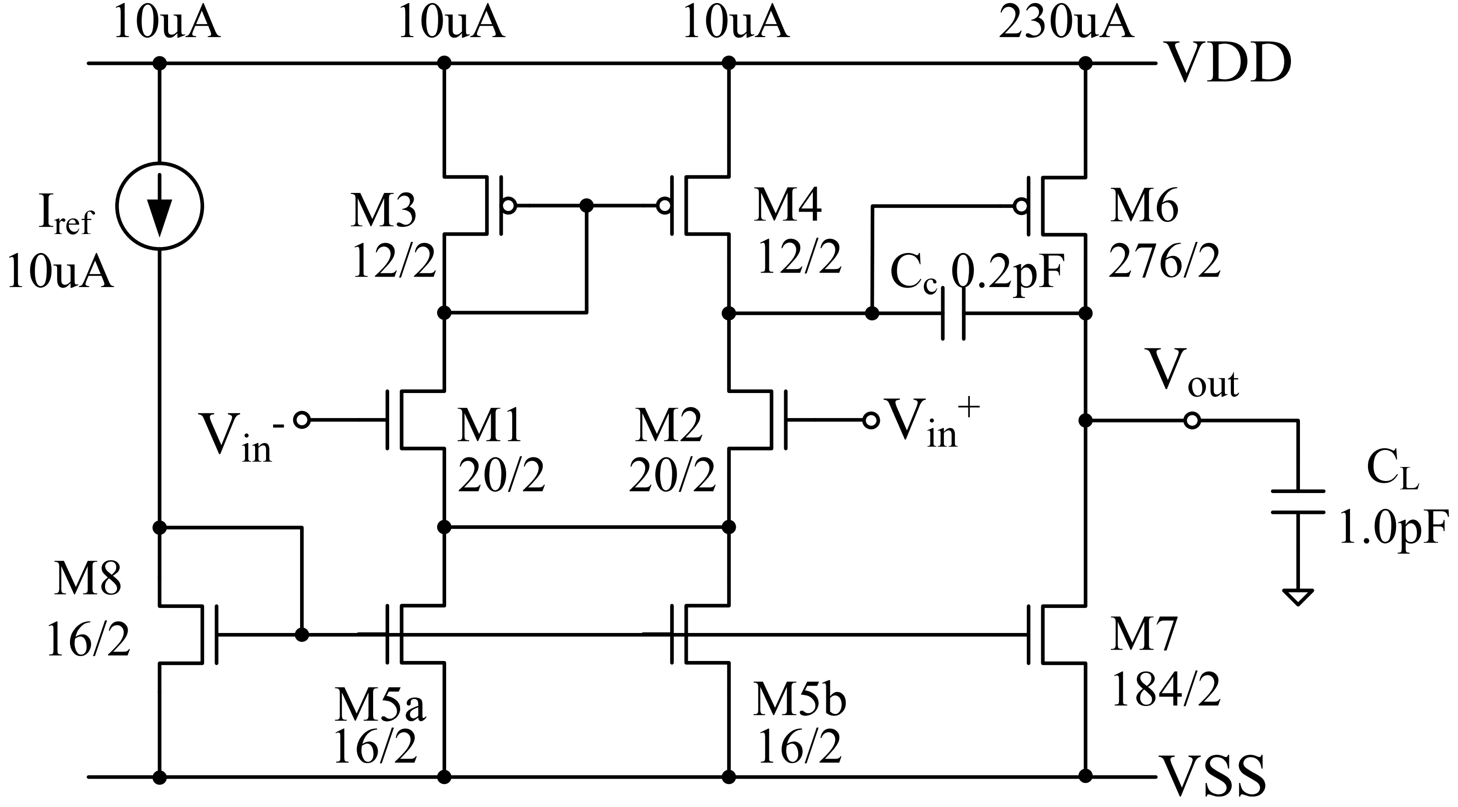
$$\begin{cases} g_{m1} = \sqrt{2\beta_1 I_{D1}} = \sqrt{2 \cdot 98\mathrm{u} \cdot 10 \cdot 10\mathrm{u}} \cong 140\mathrm{uS} \\ g_{m3} = \sqrt{2\beta_3 I_{D3}} = \sqrt{2 \cdot 33\mathrm{u} \cdot 6 \cdot 10\mathrm{u}} \cong 62.9\mathrm{uS} \end{cases}$$

at T = 300K

$$NL_t^2 = \frac{8}{3} 1.38 \cdot 10^{-23} \cdot 300 \frac{1}{140\mathrm{u}}\left(1 + \frac{62.9\mathrm{u}}{140\mathrm{u}}\right)\Delta f \le (500\mathrm{uV})^2$$

$$\Delta\mathrm{f} \le 2.187\mathrm{GHz} > 1.0\mathrm{MHz}$$

Completion



Power consumption $P_w = (230\mu + 3 \cdot 10\mu) \cdot 5.0V = 1.3$ mW