5.1 CMOS process

Overview of CMOS process
5.1.1 Structure of CMOS LSI
CMOS

- Complementary Metal-Oxide-Semiconductor process flow is complicated, but CMOS circuits have a number of advantages as follows.
  - Low power consumption
  - High speed
  - High reliability (Less malfunction)
  - Small area of MOSFET

Symbol of inverter

CMOS implementation of inverter
Structure of CMOS inverter

- A n-ch MOSFETs and A p-ch MOSFETs are integrated on a wafer.
  - A MOFET is formed in a well (or a tub).
- Electrical isolation between MOSFETs
  - STI (Shallow Trench Isolation) prevents the channel generating between MOSFETs.
  - A reverse bias between a n-well and a p-well provides an electrical isolation.

Schematic of CMOS inverter

* A silicon wafer is called a substrate of IC.
Terms
- n+ and p+ (diffusion) = Heavy doped semiconductor region
- Poly-Si or Gate poly = Gate electrode
- Contact = Electrode between a silicon and a metal
- VIA = Interconnect between metal layers
- Well = n-type or p-type semiconductor region of a body area

See section 5.1.3 for the details.
A database including a symbol, a schematic, a layout, logic function, and electrical properties such as propagation delay is called a cell library. A cell library is CAD software such as cell library is used in logic synthesis and place-and-rout.
Structure of Si wafer

- **Bulk Polished Silicon Wafer**
  - Silicon (600~900um)

- **Epitaxial Silicon Wafer**
  - Epitaxial Layer (0.5~4um)
  - Silicon (600~900um)

- **SOI Wafer** (Silicon On Insulator)
  - Silicon (50~200nm)
  - Silicon Dioxide (SiO2) (50~200nm)
  - Silicon (600~900um)
SOI (Silicon on Insulator) wafer

- Advantages of SOI structure
  - No well necessary for isolation between MOSFETs
  - High voltage operation
  - High speed (small parasitic)
Well

- **n-well (Single well)**
  (The n-ch MOSFET is fabricated on the p-substrate.)

- **Twin-well**
  (The p-wells are not isolated.)

- **Triple-well**
  (The deep n-well isolates the p-wells.)
Isolation

Field Oxide (FOX): Thickness = 100nm
Gate Oxide (GOX): Thickness = nanometer scale

- The thick SiO₂ of FOX prevents the channel generating.
- The thin SiO₂ of GOX can produce the channel.

* FOX is formed by STI (Shallow trench isolation) process (described below)
** High-k dielectrics are used in advanced technology where they are usually used to replace a silicon dioxide gate dielectric.
5.1.2 LSI process
Advantages of single crystal Si

• Low cost
  – Main constituent elements of the earth
  – Low production cost

• Easy processing
  – Easy to purify (Si atoms are strongly bonded together.)
  – Large-diameter single crystal(*)
  – High mechanical strength
  – High melting point ~1410 degrees Celsius

• Good homogeneity
  – Highly level of uniformity of MOSFET characteristics

  • Single crystal: A material in which the crystal lattice of the entire sample is continuous and unbroken to the edges of the sample, with no grain boundaries.
Outline of process flow

Si wafer

Microfabrication (微細加工)

Test (良品選別)

Dicing (チップ切断)

Packaging

Design data

Photomask

Photomask (Reticle): an opaque plate with holes or transparencies that allow light to shine through in a defined pattern. They are commonly used in photolithography.
The circuit simulation or the electromagnetic field analysis of the chip including the package is performed for the high-speed or RF IC.

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Name</th>
<th>Pictures</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIP</td>
<td>Dual in-line package</td>
<td><img src="image" alt="DIP" /></td>
</tr>
<tr>
<td>SOP</td>
<td>Small out-line package</td>
<td><img src="image" alt="SOP" /></td>
</tr>
<tr>
<td>SOJ</td>
<td>Small out-line J-lead package</td>
<td><img src="image" alt="SOJ" /></td>
</tr>
<tr>
<td>QFP</td>
<td>Quad flat package</td>
<td><img src="image" alt="QFP" /></td>
</tr>
<tr>
<td>PGA</td>
<td>Pin grid array</td>
<td><img src="image" alt="PGA" /></td>
</tr>
<tr>
<td>BGA</td>
<td>Ball grid array</td>
<td><img src="image" alt="BGA" /></td>
</tr>
<tr>
<td>CSP</td>
<td>Chip size package</td>
<td><img src="image" alt="CSP" /></td>
</tr>
</tbody>
</table>
Photolithography

• The mask features are on a larger scale (e.g. 4X or 10X) relative to the features exposed on the wafer surface.
• The reduced size projection is accomplished with a projection stepper.
Stepper

- The pattern of the chip is transferred, and the array of the chip is formed on the entire surface of the wafer by step-and-repeat method.
Principle of microfabrication 1

- Backend-of-the-line (Interconnect)

- Pre-metal dielectric deposition
- Metal film deposition
- Photoresist coating
- UV irradiation through photomask
- Developing (Metal definition by the photoresist pattern)
- Metal etching by reactive ion
- Photoresist plasma ashing

Complete
Principle of microfabrication 2

- Frontend-of-the-line (pn junction)

- Dielectric deposition
- Photoresist coating
- UV irradiation through photomask
- Developing (n+ definition)
- Dielectric etching by reactive ion
- Photoresist plasma ashing
- Ion implantation
- Annealing (Impurity activation)

Complete
5.1.3 CMOS Process integration
Design example of inverter

Layout:
- **IN**
- **OUT**
- **VDD**
- **GND**

Cross section:
- Interlayer dielectric
- **metal-1**
- **GOX (Gate oxide)**
- **poly-1**
- **via-1**

Twin well process:
- **n-well**
- **n-active (n+)**
- **p-active (p+)**
- **poly-1**
- **contact**
- **metal-1**
- **via-1**
- **metal-2**

Details:
- **VDD**
- **STI (Shallow trench isolation)**
- **n+**
- **p+**
- **p-well**
- **p+ substrate**
- **n-well**
- **p-**
Shallow trench isolation module 1

Process flow

p-/p+ Epitaxial grown layer on bulk Si (p-Si),
Deposition of Si₃N₄/SiO₂
(The SiO₂ is thermally grown.)

Active area definition by Si₃N₄/SiO₂
Shallow trench isolation module 2

Timed silicon trench outside of Si$_3$N$_4$/SiO$_2$ by reactive ion etching

SiO$_2$ deposition
Shallow trench isolation module 3

Removal of Si$_3$N$_4$/SiO$_2$ using CMP (Chemical-Mechanical Polishing)

Si$_3$N$_4$/SiO$_2$ etching
STI (Shallow Trench Isolation) is formed.
n-well definition by photoresist, Phosphorus implantation, Photoresist plasma ashing, Drive-in diffusion of phosphorous, p-well formation in the same way of n-well

Gate dielectric (GOX) formation using dry oxidation
Gate module

Polysilicon deposition

Gate electrode and local interconnect photolithography and polysilicon reactive ion etching
Source/Drain module

As (Arsenic)

n+ source/drain formation using a low energy, high dose implantation of As

The polysilicon blocks the implantation, and automatically source and drain are formed on both side of the gate (Self-Alignment process)

BF₂ (Boron fluoride)

p+ source/drain formation using a low energy, high dose implantation of BF₂
Self-aligned silicide module

Removal of the oxide on the source and the drain, Ti（チタン）deposition

Low resistivity TiSi₂（チタン・シリサイド）is formed by RTA (Rapid thermal annealing), Removal of Unreacted Ti, Self-aligned silicide = Silicide process
Pre-metal dielectric

SiO₂ or PSG (Phosphosilicate glass) deposition, This layer is called PMD (Pre-metal Dielectric).

Planarization using CMP (Chemical-Mechanical Polishing)
Contact module

Opening contact hole in the PMD layer

W（タンゲステン） deposition
Metallization 1

W CMP to form defined contacts

Metal-1 stack deposition (Ti/TiN/AlCu/TiN)
Intra-metal dielectric 1 deposition

Metal-1 definition using photolithography and dry metal etch

SiO₂ or BPSG (Boron-phosphoresce silicate glass) deposition (IMD: Intra-metal Dielectric), Planarization using CMP
Via 1 module

Via-1 definition using photolithograph and dry IMD etch

W via fill deposition
Metallization 2

W CMP to form defined vias

Metal-2 stack deposition (Ti/TiN/AlCu/TiN)
Final passivation

Metal-2 definition using photolithography and dry metal etch

Deposition of passivation layer, Bond pad definition using dry etch of passivation film.

The actual process is more complicated in order to improve the electrical reliability.
Profile of impurity concentration

The depth of pn junction is controlled by an acceleration energy of ion implantation and a time of drive-in diffusion.

\[ N_{\text{eff}} = N_D - N_A \]

- \( N_A \): Concentration of accepters
- \( N_D \): Concentration of donors

If both impurities of donor and accepter are doped,
- If \( N_{\text{eff}} > 0 \), then n-type
- If \( N_{\text{eff}} < 0 \), then p-type
- If \( N_{\text{eff}} = 0 \), then pn junction
5.1.4 Interconnect
Multilayer interconnection

- **Top metal**
  - Bond pad

- **Global**
  - Data BUS,
  - Clock,
  - Power supply

- **Intermediate**
  - Connecting path between the intermediate layer and the global layer
  - Interconnects inside the circuit module and connection between circuits

- **Semi-global**

- **Local**
  - Interconnects inside the cell (gate)

**Example of 12-layer interconnect**

Electron micrograph of cross section
Resistivity of metals

\[ R = \rho \frac{L}{t \cdot W} \]

\[ E(V/m) = \rho(\Omega m)J(A/m^2) \]

<table>
<thead>
<tr>
<th>Material</th>
<th>Al</th>
<th>Cu</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resistivity ( \rho )</td>
<td>3.3 ( \mu \Omega ) cm</td>
<td>2.23 ( \mu \Omega ) cm</td>
</tr>
</tbody>
</table>

Advantages of Cu wire

- Low resistivity
- High maximum current density

0.2\( \mu \)m Cu interconnect (Source: IBM)
Dual damascene process

The performance of Cu wire is higher than the wire of Al, however, it is hard to process Cu wires by dry etching. The embedded Cu wire is formed by the dual damascene process.

![Diagram showing the dual damascene process]

Barrier metal (Ta or TaN): The barrier metal prevent the diffusion of Cu atoms into IMD.

* CMP (Chemical Mechanical Polishing:化学機械的研磨)