2.2 CMOS static logic gates

The design of primitive logic gates
CMOS

CMOS = Complementary MOS

This term has two meanings.

- The process technology to integrate p-ch MOSFETs and n-ch MOSFETs
- The circuit structure with p-ch MOSFETs and n-ch MOSFETs
MOSFET switch

MOSFET symbol with 3 terminals

MOSFET symbol with 4-terminals

V_G = Low
V_G = High

Analogy of switch
# Primitive logic gates

<table>
<thead>
<tr>
<th>Combinational logic</th>
<th>Sequential logic</th>
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<tbody>
<tr>
<td>1 stage</td>
<td>2 stages</td>
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<tr>
<td><img src="image1" alt="Gate1" /></td>
<td><img src="image2" alt="Gate2" /></td>
</tr>
</tbody>
</table>
Inverter

Truth table

<table>
<thead>
<tr>
<th>IN</th>
<th>OUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

The terminal of OUT is switched to VDD or GND.
The MOSFET cannot turn on the GND. A p-ch MOSFET can output VDD.

The MOSFET cannot turn on the VDD. A n-ch MOSFET can output GND.
General form of the static logic

A pull-up network is a switch network for VDD.
A pull-down network is a switch network for GND.
2-input switch networks

PUN consists of p-ch MOSFETs.

PDN consists of n-ch MOSFETs.
Function of 2-input NAND

Symbol

\[
\begin{array}{ccc}
A & B & Y \\
0 & 0 & 1 \\
0 & 1 & 1 \\
1 & 0 & 1 \\
1 & 1 & 0 \\
\end{array}
\]

de Morgan's laws

\[
Y = \overline{A} + \overline{B} \\
\Rightarrow Y = \overline{A} \cdot \overline{B}
\]

\rightarrow \quad \text{p-ch MOSFET network}

\rightarrow \quad \text{n-ch MOSFET network}

At first, find 2 equivalent Boolean expressions.

\{ (1) The expression of each variable negation
(2) The expression of the total negation

Note: If you cannot find the equivalent Boolean expressions, there is no logic circuit that consists of 1-stage.
Design of 2-input NAND

\[ Y = \begin{cases} \bar{A} + \bar{B} & \rightarrow \text{PUN} \\ A \cdot B & \rightarrow \text{PDN} \end{cases} \]

**PUN**
If \( A = 0 \) OR \( B = 0 \), then \( Y = 1 \)

**PDN**
If \( A = 1 \) AND \( B = 1 \), then \( Y = 0 \)

Connection of PUN and PDN
Function of 2-input NOR

Symbol

\[
\begin{array}{ccc}
A & B & Y \\
0 & 0 & 1 \\
0 & 1 & 0 \\
1 & 0 & 0 \\
1 & 1 & 0 \\
\end{array}
\]

Truth table

de Morgan's laws

\[
Y = \overline{A} \cdot \overline{B} \quad \rightarrow \quad p\text{-ch MOSFET network}
\]

\[
= A + B \quad \rightarrow \quad n\text{-ch MOSFET network}
\]
Design of 2-input NOR

\[ \overline{A \cdot B} \rightarrow \]

\[ \overline{A + B} \rightarrow \]
Design of AND, OR

\[
\text{AND} \rightarrow A \cdot B = \overline{A + B} \\
\text{OR} \rightarrow A + B = \overline{A \cdot B}
\]

PUN and PDN cannot build the operations shown above.

\[
\text{AND operation and OR operation require 2 stage(\text{*}) logic circuits.} \\
\text{1-stage + 1 stage}
\]

* Stage: 段数
Multi-input gates

\[ Y = \overline{A} + B + \overline{C} + \overline{D} \]

\[ = A \cdot B \cdot C \cdot D \]

Too much number of inputs causes a delay times, because the n-ch MOSFETs connected in series reduce the current flowing to GND.

DO not over 4-input.
8-input NAND

\[ Y = A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H \]
\[ = (A \cdot B \cdot C \cdot D) \cdot (E \cdot F \cdot G \cdot H) \]
\[ = A \cdot B \cdot C \cdot D + E \cdot F \cdot G \cdot H \]

de Morgan's laws

1 stage + 2 stages
8-input AND

\[ Y = A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H \]
\[ = (A \cdot B \cdot C \cdot D) \cdot (E \cdot F \cdot G \cdot H) \]
\[ = A \cdot B \cdot C \cdot D + E \cdot F \cdot G \cdot H \]

de Morgan's laws

\[ Y = \overline{A \cdot B \cdot C \cdot D} + \overline{E \cdot F \cdot G \cdot H} \]

1 stage + 1 stage
Counting method of gate stages

- A number of stages is defined as a maximum number of gate electrodes of MOSFET on the path from an input port to an output port.

Example of 2-stage gate
Propagation delay

- A propagation delay (伝搬遅延時間) is defined as a time between 50% points of input and output.
- The propagation delay $t_{logic}$ of the logic circuit is estimated from the number of stages $K$ and the propagation delay $t_d$ of 1-stage gate.

$$t_{logic} = K \cdot t_d$$
3-input AND-NOR gate 1

\[ Z = (A \cdot B) + C \]

Construction by PUN and PDN

10 MOSFETs

3 stages

AND-NOR and OR-NAND are also called a complex gate (複合ゲート).
3-input AND-NOR gate 2

\[ Y = \overline{(A \cdot B) + C} \]
\[ = A \cdot B \cdot \overline{C} \quad \text{de Morgan's laws} \]
\[ = (\overline{A + B}) \cdot \overline{C} \]

\[(A + B) \cdot \overline{C} \]

\[(A \cdot B) + C \]

6 MOSFETs, 1 stage
3-input OR-NAND gate 1

\[ Y = (A + B) \cdot C \]

Construction by PUN and PDN

10 MOSFETs

3 stages
3-input OR-NAND gate 2

\[ Y = \overline{(A + B) \cdot C} \]
\[ = A + B + \overline{C} \]
\[ = (\overline{A \cdot \overline{B}}) + \overline{C} \]

de Morgan's laws

\((A \cdot \overline{B}) + \overline{C}\)

\((A + B) \cdot \overline{C}\)

6 MOSFETs, 1 stage